

ZZZ2
PCB
M/B
DAZ@

ZZZ1
LA-7072P
M/B
DA@

ZZZ3
LS-7072P
LED/B
DA@

ZZZ4
LS-7073P
TP/B
DA@

11/18
LA-7072P P/N from DA60000LA00 to DA60000LA10
LS-7072P P/N from DA40000Z300 to DA40000Z310
LS-7073P P/N from DA40000Z400 to DA40000Z410

11/22
LS-7073P P/N from DA40000Z410 to DA20000Z410

11/18 ZZZ2 for DAZ P/N:DAZ0IV00101

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P0VE6 LA7072P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

10.1" M/B

2010-11-18

Rev : 1.0

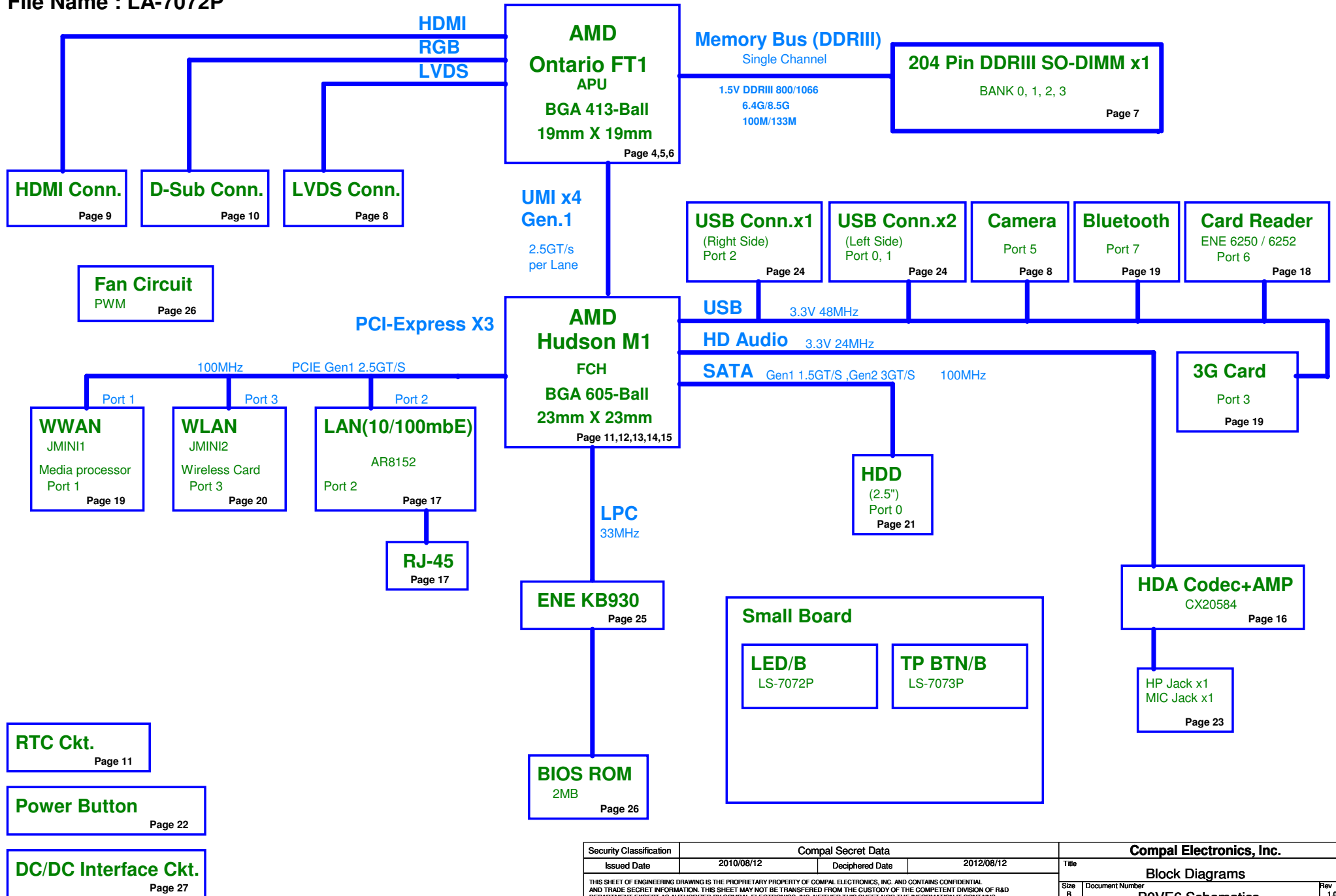
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Model Name : P0VE6 / P0VH6

File Name : LA-7072P

Brazos Platform



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	SB-TSI	1001-100xb	98H

SM Bus Controller 0		
	(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)	
Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1		
	(FCH_SMB0)	
Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

BOM Structure

HDMI@ : HDMI function
BT@ : BT function
CONN@ : Conneters
45@ : 45 Level
3G@ : 3G function
3G_MP@: 3G & Media processor function
CHARGE@: Charge BATT
NONCHARGE@: nonCharge BATT

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB2
Port1	Right USB3
Port2	Left USB1
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	NC
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

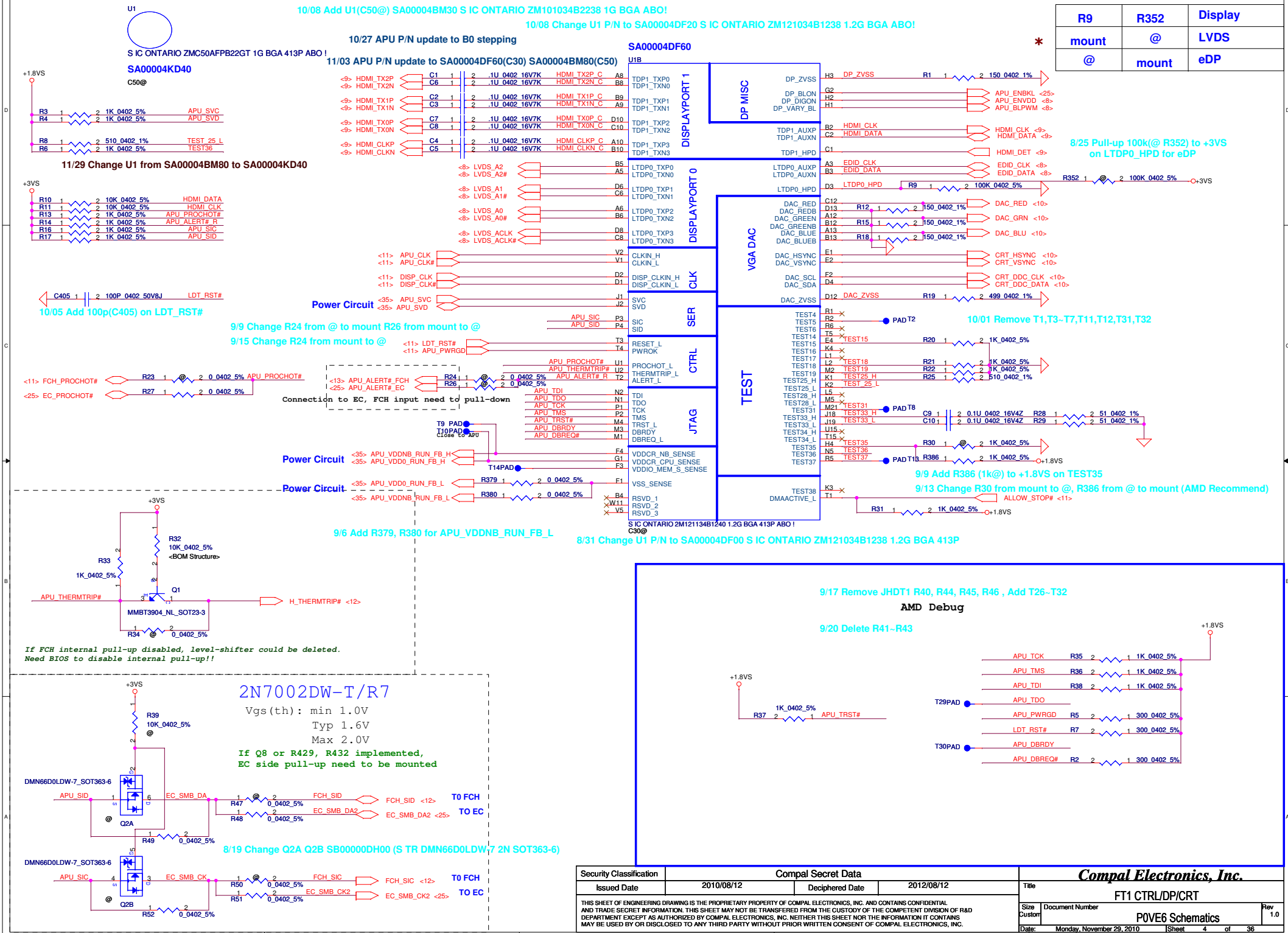
Board ID / SKU ID Table for AD channel

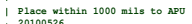
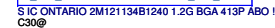
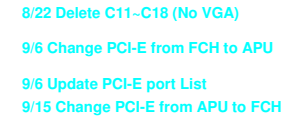
Vcc	+3VALW				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

SMBUS Control Table

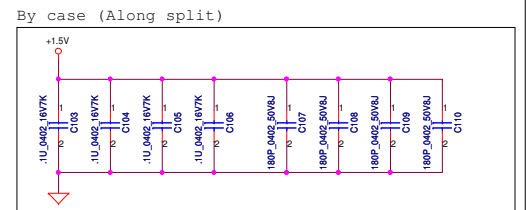
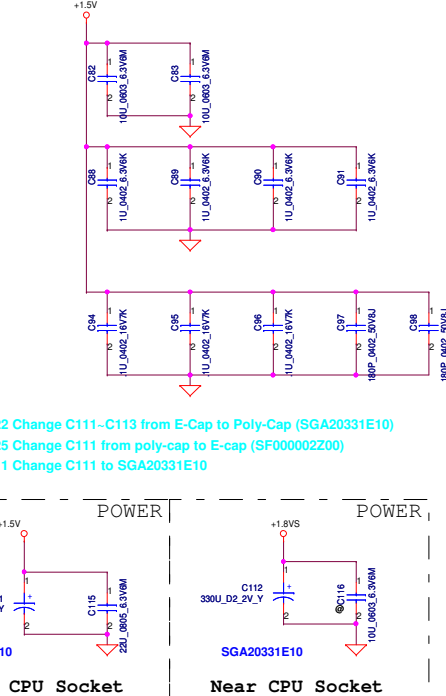
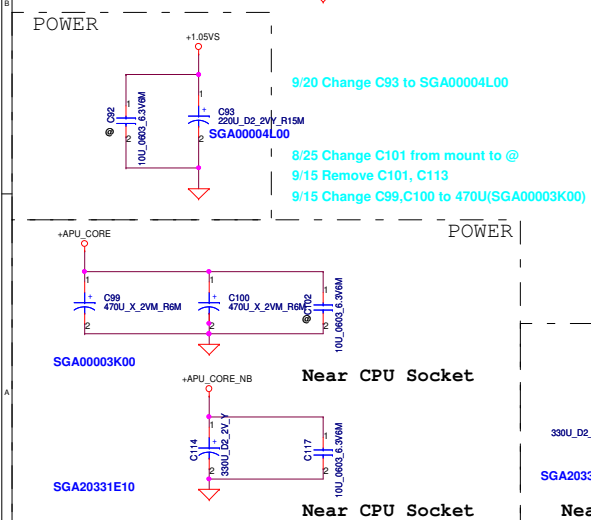
	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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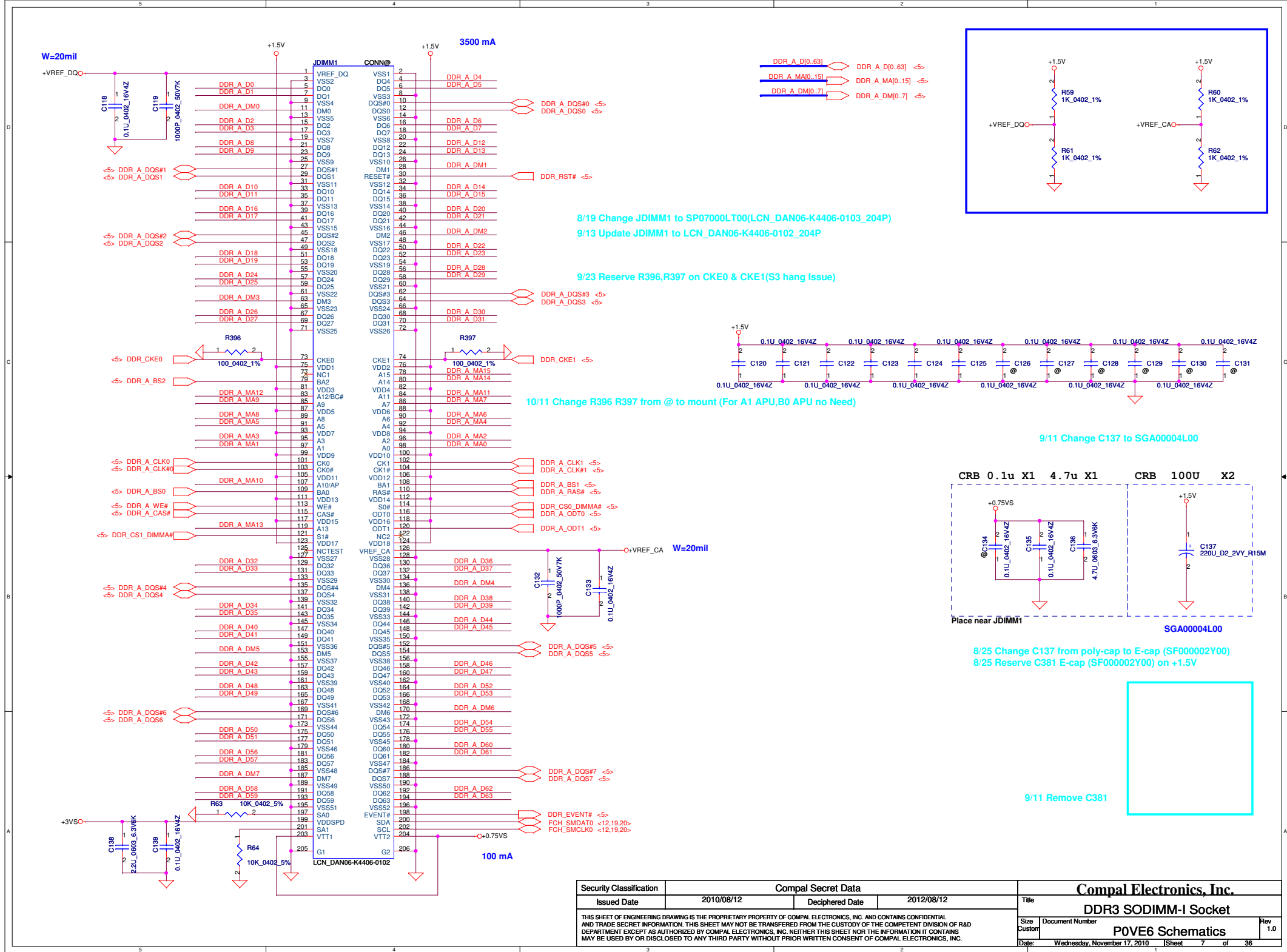




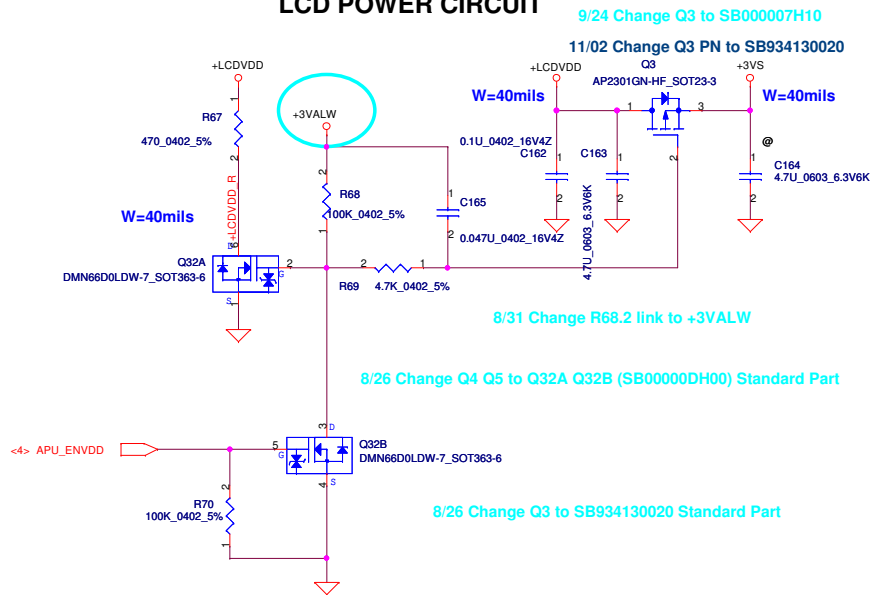
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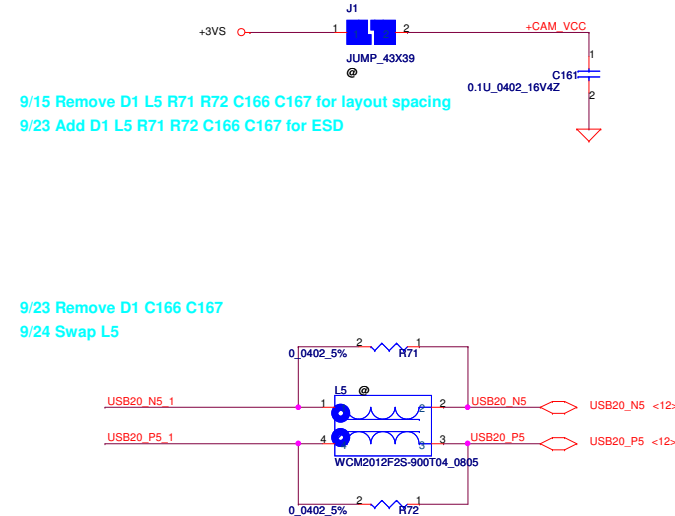
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LCD POWER CIRCUIT



About Camera



9/9 Reserve 100k PD to GND on INVT PWM 9/17 Change R387 from @ to mount

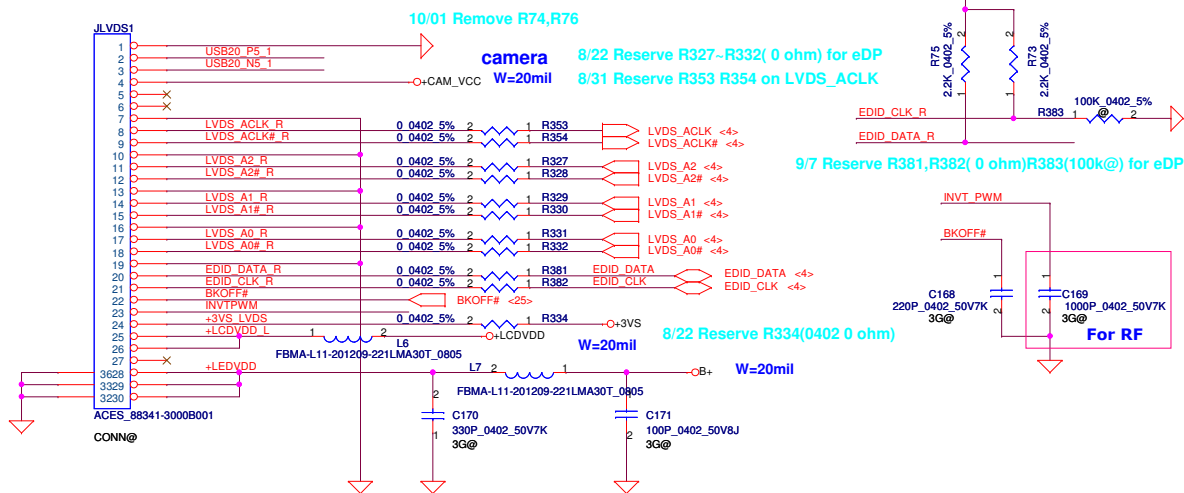
CMOS & LCD/PANEL BD. Conn.

8/25 JLVDS1.5 change to INT_MIC0 JLVDS1.6 change to GNDA

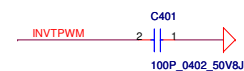
8/31 Update JLVDS1 Pin definition Delete R74 R76

9/13 Update LVDS Pin definition, Add R74,R76

9/13 Add Net Name +3VS_DMIC



10/04 Add 100p(C401) on INVT_PWM

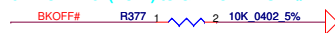


10/04 Change C401 on INVT PWM

*

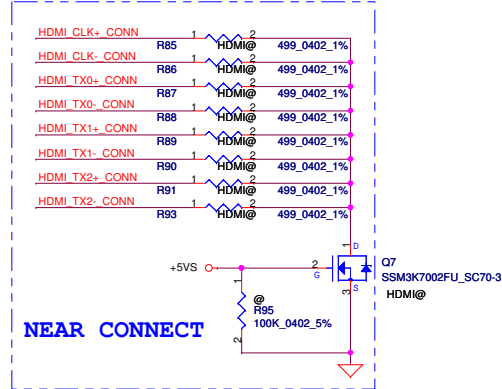
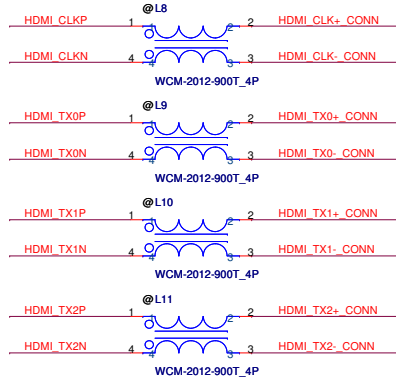
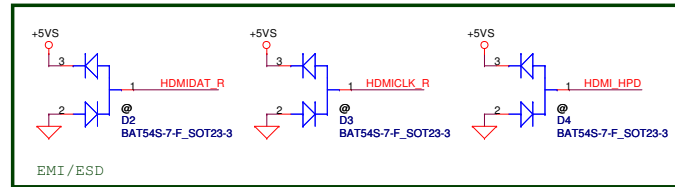
Display	LVDS	eDP
R331	0 ohm	0.1uF
R332	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

9/3 Pull-Down 10k(R377) to GND on BKOFF#



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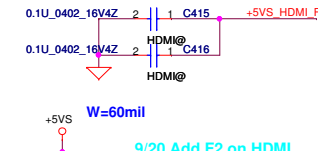
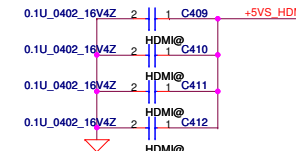
<4> HDMI_CLKP R77 1 HDMI@ 2 0.0402 5% HDMI_CLK+ CONN
<4> HDMI_CLKN R78 1 HDMI@ 2 0.0402 5% HDMI_CLK- CONN
<4> HDMI_TX0P R79 1 HDMI@ 2 0.0402 5% HDMI_TX0+ CONN
<4> HDMI_TX0N R80 1 HDMI@ 2 0.0402 5% HDMI_TX0- CONN
<4> HDMI_TX1P R81 1 HDMI@ 2 0.0402 5% HDMI_TX1+ CONN
<4> HDMI_TX1N R82 1 HDMI@ 2 0.0402 5% HDMI_TX1- CONN
<4> HDMI_TX2P R83 1 HDMI@ 2 0.0402 5% HDMI_TX2+ CONN
<4> HDMI_TX2N R84 1 HDMI@ 2 0.0402 5% HDMI_TX2- CONN



8/26 Change Q7 to SB000009610 Standard Part

10/29 Add C409~C412(0.1U) on +5VS_HDMI

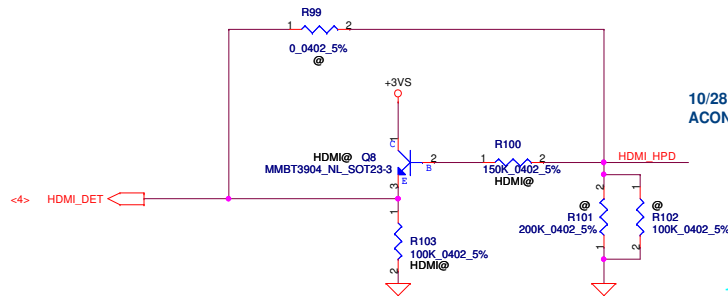
10/29 Add C415~C416(0.1U) on +5VS_HDMI_F



10/27 Change D5 P/N from SC1B491D000 to SCS00003H00

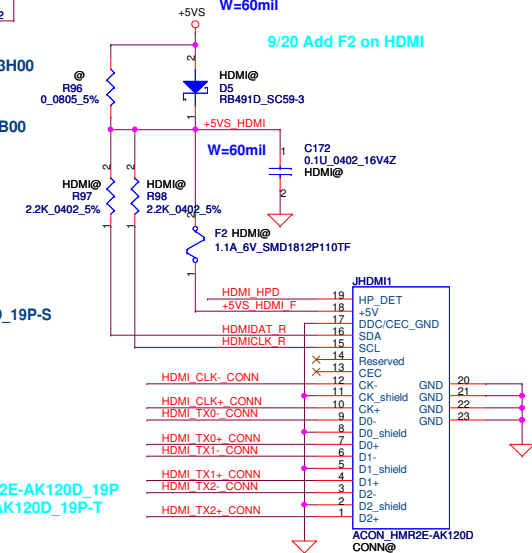
10/27 Change F2 P/N from SP04301P120 to SP040001B00

9/20 Change R99 from HDMI@ to @
9/20 Change Q8,R100 from @ to HDMI@



10/28 Change JHDMI1 footprint from ACON_HMR2E-AK120D_19P-T to ACON_HMR2E-AK120D_19P-S

10/07 Update JHDMI1 footprint from ACON_HMR2E-AK120D_19P to ACON_HMR2E-AK120D_19P-T



8/23 Update JHDMI1 Symbol (SUYIN_100042GR019S268ZR_19P-T)

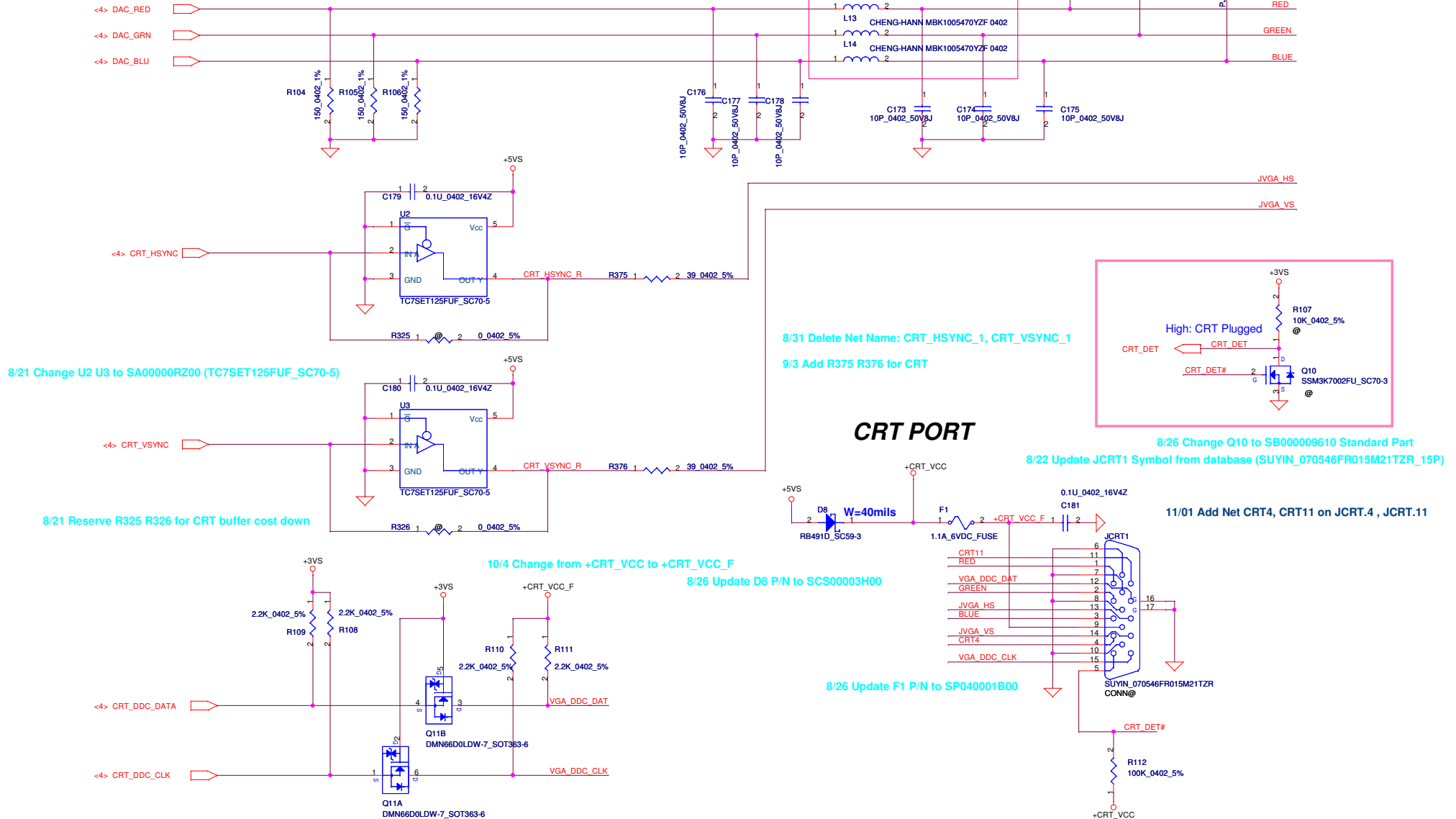
8/23 Update JHDMI1 Symbol (SUYIN_100042GR019M23DZL_19P-T)

9/7 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)

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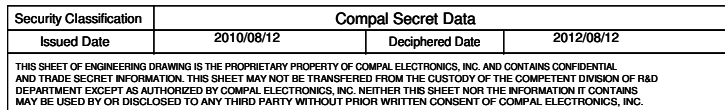
Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

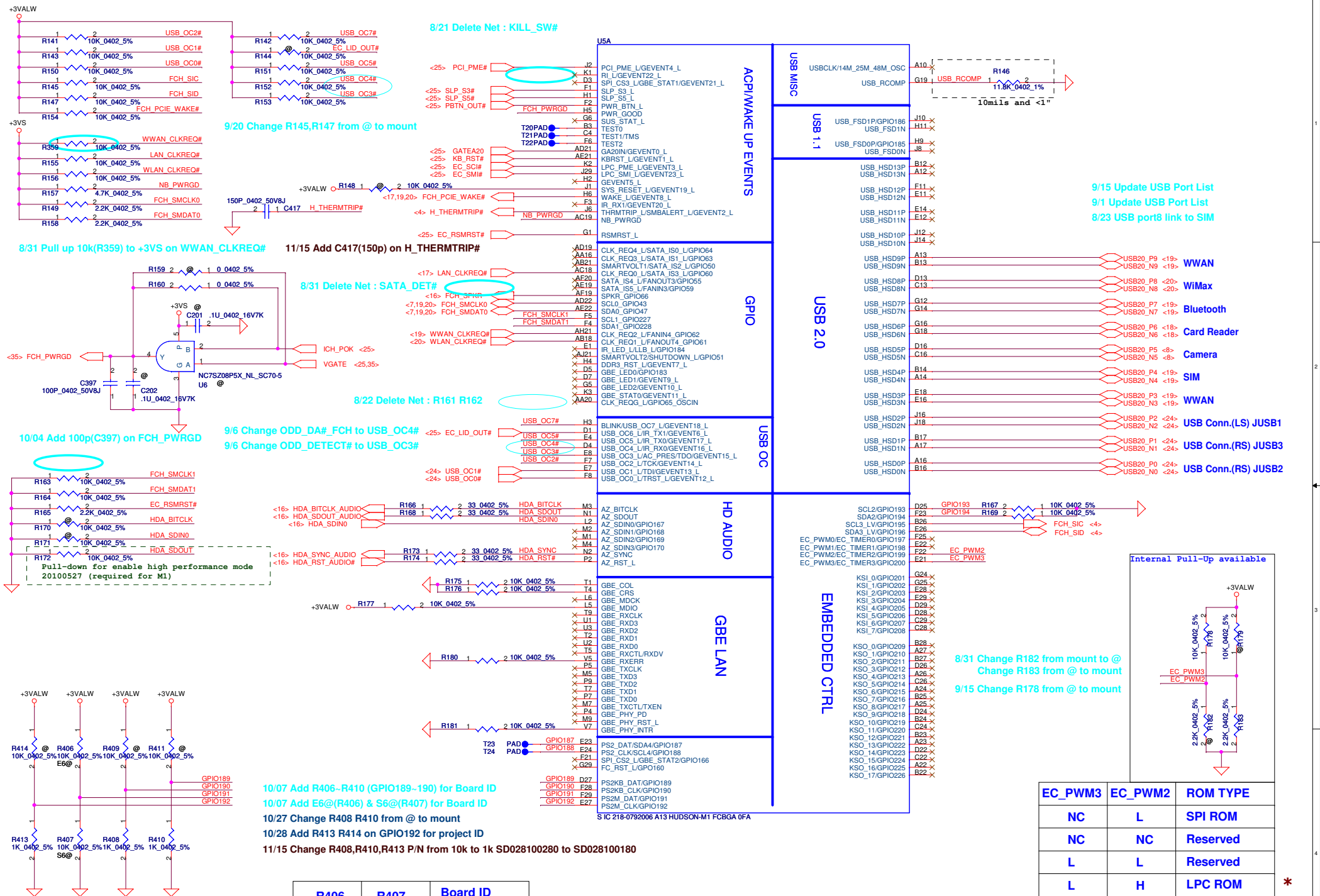
Change L12. L14, L15 to SM01000C600 2010/04/06



8/19 Change Q11A Q11B to SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

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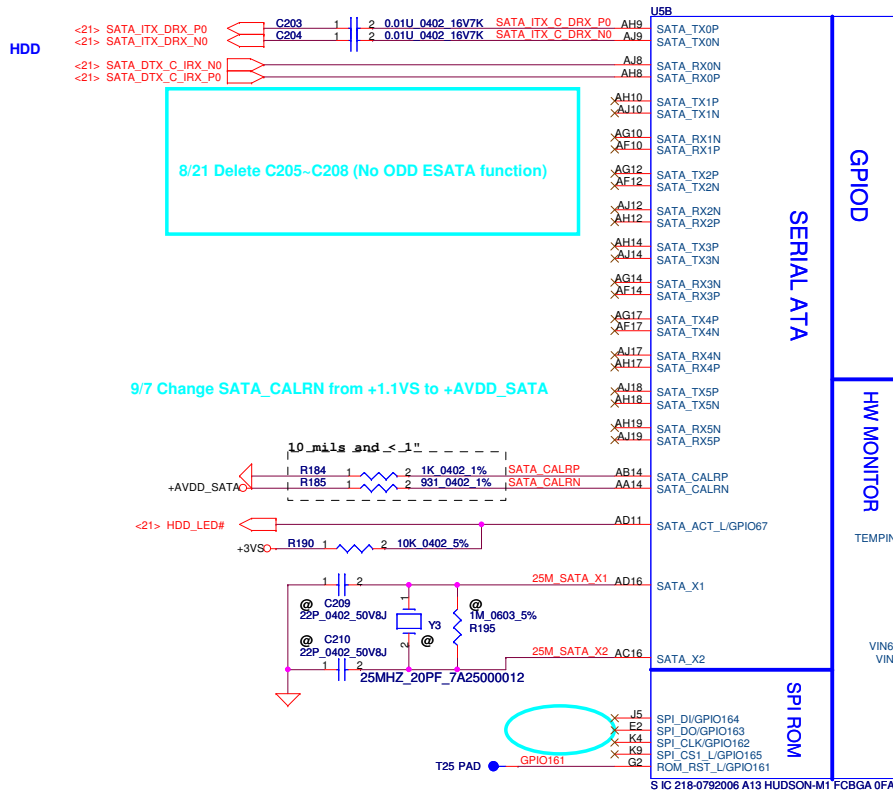


R406	R407	Board ID
mount	@	P0VE6
@	mount	P0VS6

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EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM

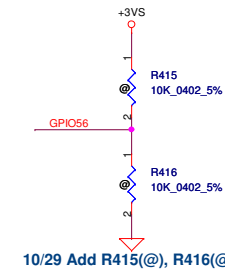
Compal Electronics, Inc.		
FCH HDA/USB/ACPI		
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11/01 Add Net U5_AE29 on U5.AE29

11/15 Delete net U5_AE29

8/21 Delete Net : ODD_EN
8/22 Delete Net : BT_OFF#, WL_OFF#

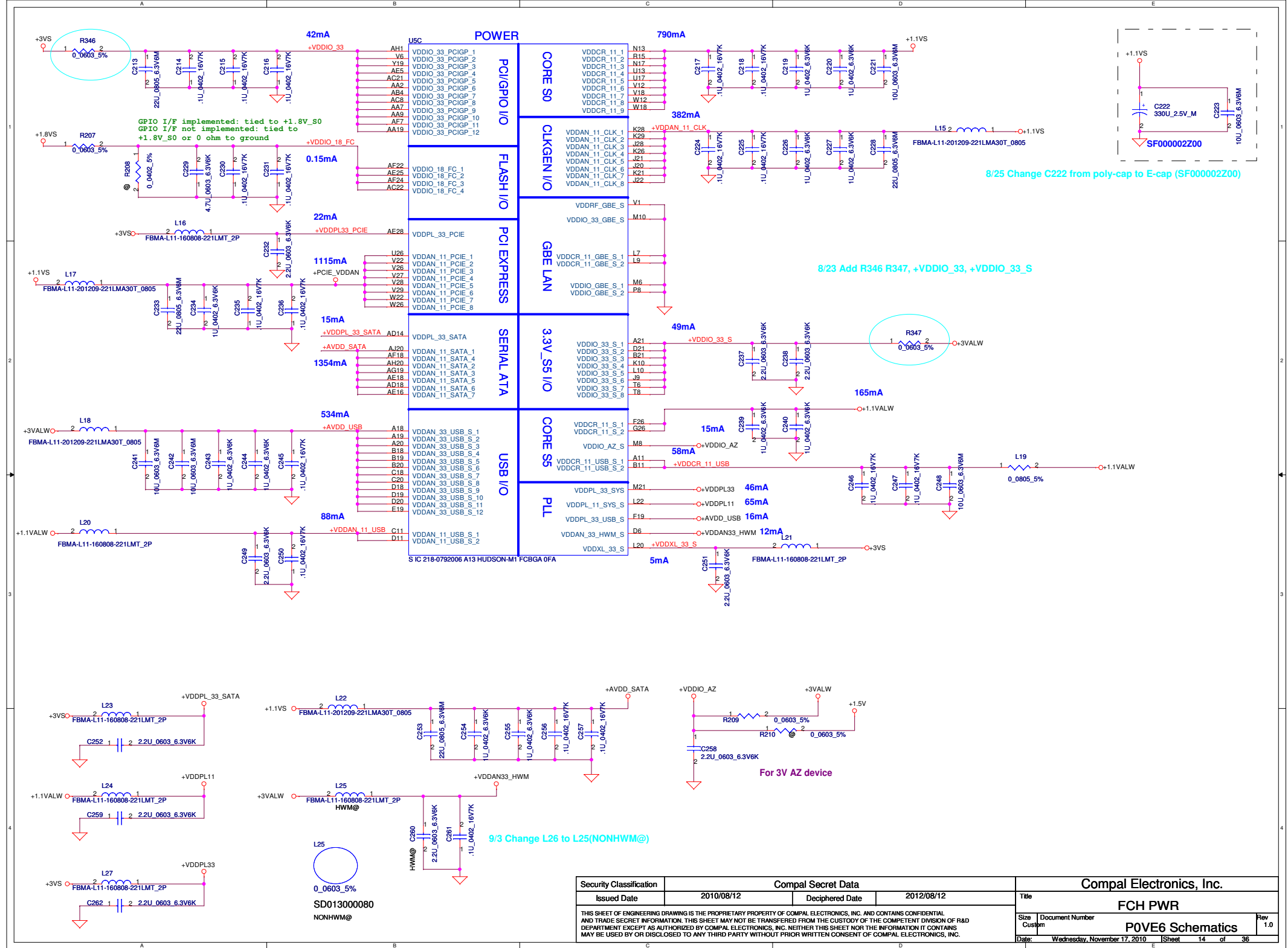


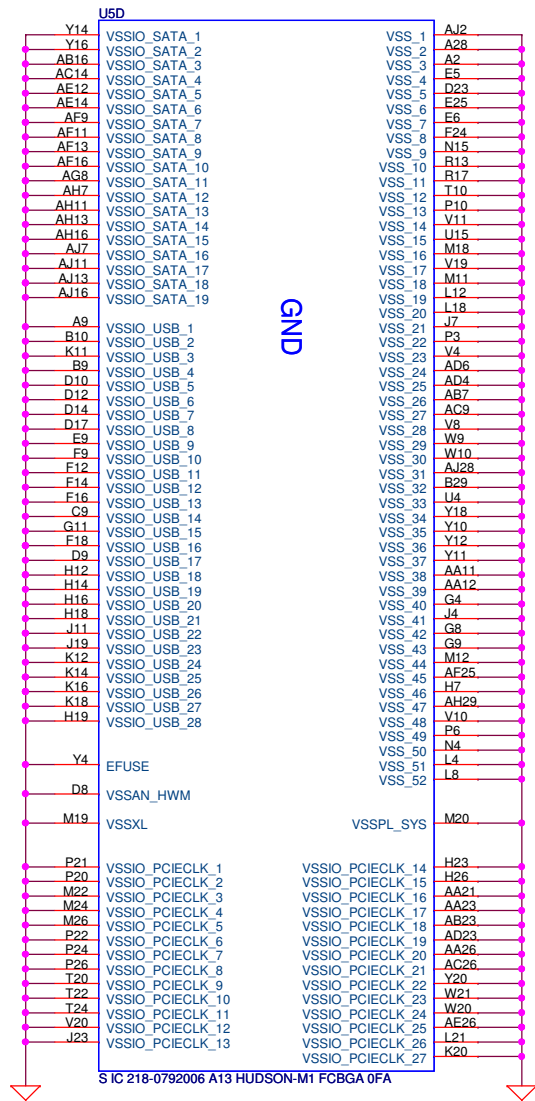
9/9 Change R189 from mount to @
9/15 Change R189 from @ to mount

VIN6/GBE_STAT3/GPIO181
Enable integrated pull-down/up and leave unconnected

C406 1 2 100P 0402 50V8J APU_ALERT#_FCH
10/05 Add 100p(C406) on APU_ALERT#_FCH

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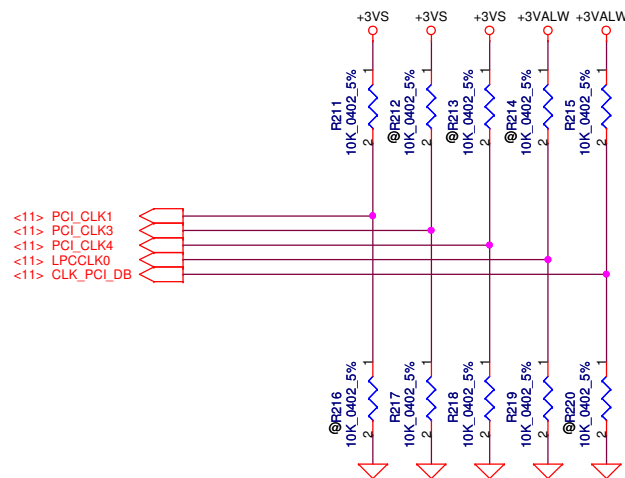




REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 ★	USE DEBUG STRAP	Reserved	Internal EC ENABLE	Internal CLKGEN Mode ★				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP ★	CLKGEN Mode Internal ★	Internal EC DISABLE ★	External CLKGEN Mode				



9/13 Change R211 from mount to @, R216 from @ to mount

9/13 Change R211 from @ to mount, R216 from mount to @

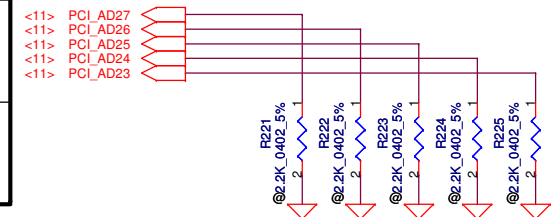
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK ★	ILA AUTORUN Disabled ★	Selects FC PLL ★	Disable I2C ROM ★	Required Setting ★
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default



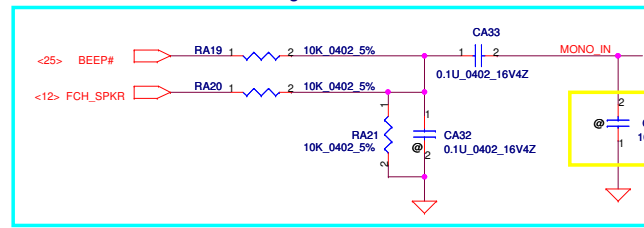
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				Size B	Document Number	Rev 1.0
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Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
 Port B: Internal MIC (mono or stereo)
 Port C: Microphone/LI/LO jack
 Port D: Line Out jack (Optional)
 Port E: Line In jack (Optional)
 Port F: Not used.
 Port G: Internal stereo speakers
 Port J: Internal stereo digital mic (Optional)
 Port H: S/PDIF (jack shared with headphone)

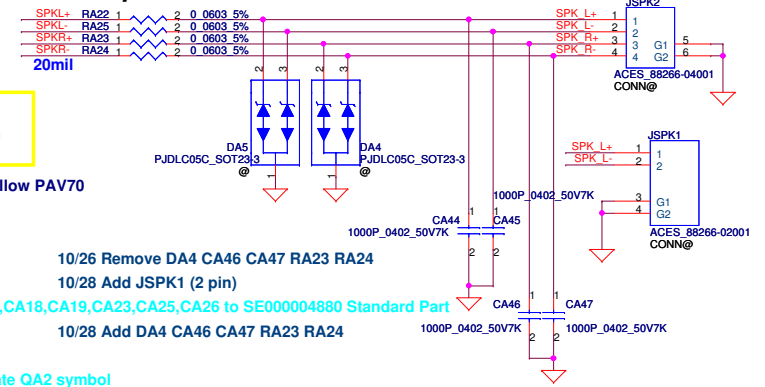
08/19 Follow NTUC0

11/04 Change RA19 RA20 from 47k to 10k

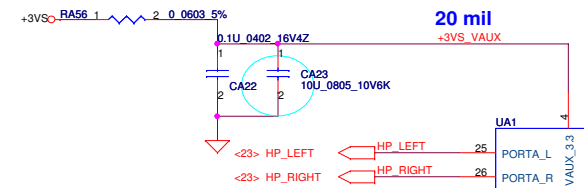


08/21 Follow PAV70

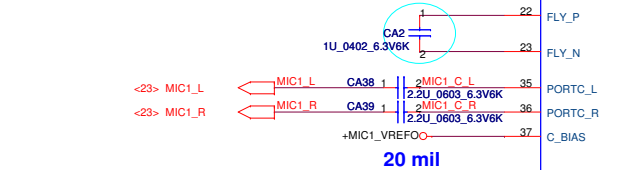
Int. Speaker Conn.



9/3 Change CA38~ CA43 from 4.7u to 2.2u
 Change RA16 from 1k to 100 ohm

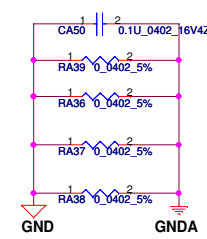


9/3 Change RA17 from 1k to 0 ohm



11/17 Change RA33 from mount to @

9/7 Add 0.1u (CA50) between GND & GNDA



08/25 Change CA1,CA2,CA3,CA4 to SE00000K80 Standard Part

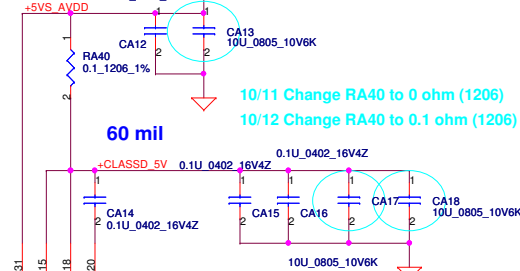
SA000034010

08/25 Add UA1 PN:SA000034010

10/11 Update UA1 PN:SA000034020

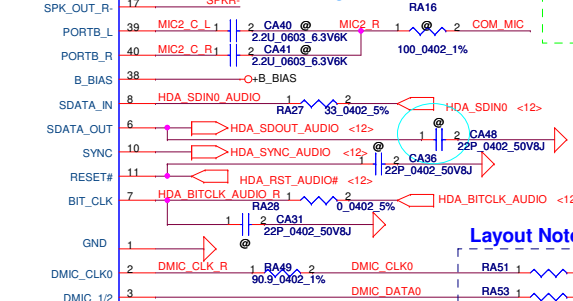
10/12 Update UA1 PN:SA000034010

9/25 Add RA54~RA56



10/26 Remove SPKR+ SPKR- function

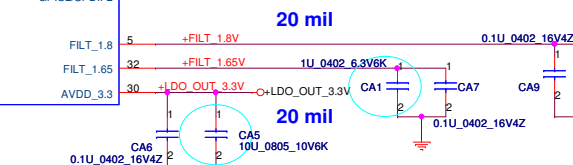
11/17 Change CA40,CA41,RA16 from mount to @



9/6 UA1 Pin 1 link to GNDA

9/7 Change UA1 Pin1 to GND

9/13 Add RA49 for DMIC

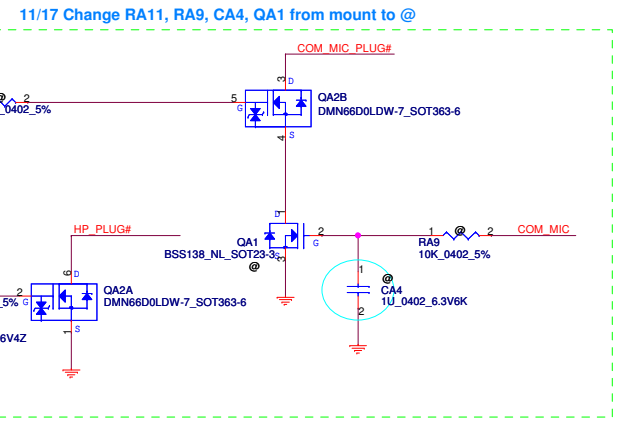


Layout Note: close to UA1

9/13 Add RA50~RA53 for DMIC

10/01 Remove RA50,R52

9/6 Update QA2 symbol
 Combo Jack



9/1 Add CA49 RA41 on HP_SENSE

08/31 Reserve CA48(22P) on HDA_SDOOUT_AUDIO

10/28 Reserve CA57 CA58 for EMI

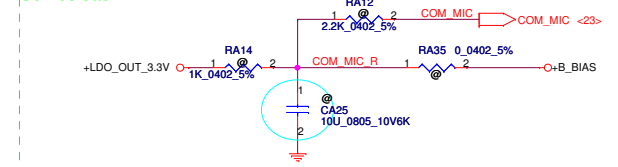
11/01 Change CA57, CA58 from @ to mount



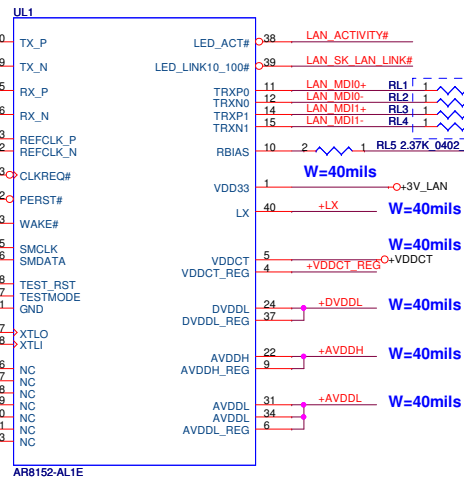
9/13 Remove Analog MIC circuit

11/17 Change RA12,RA14,CA25 from mount to @

Combo Jack

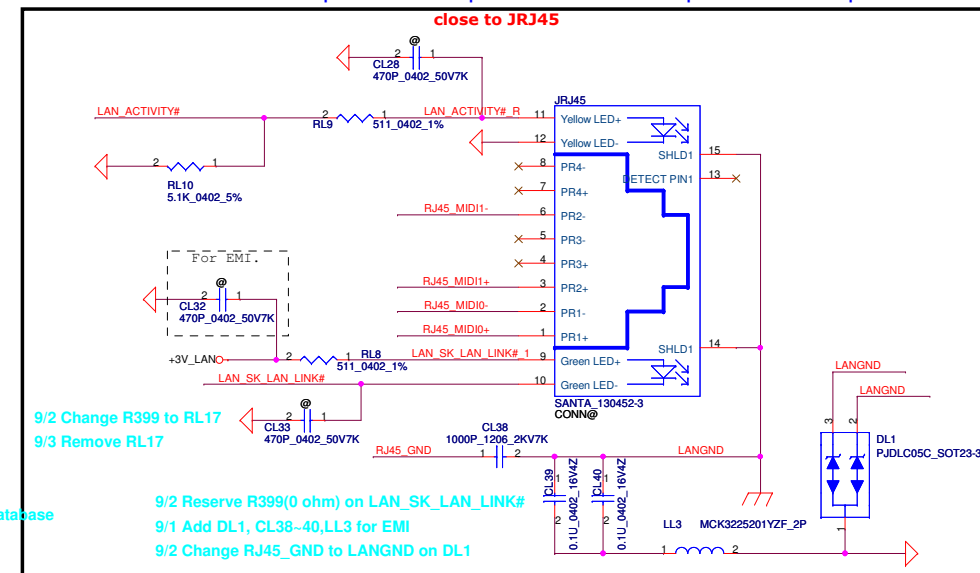
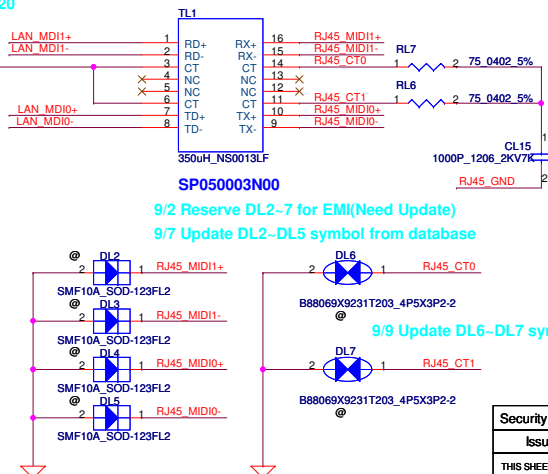
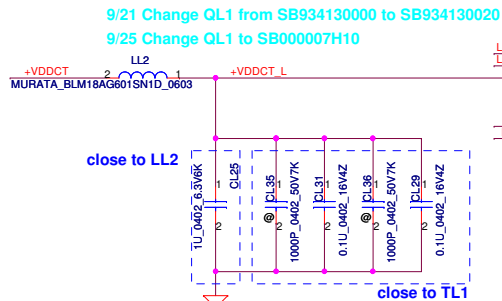
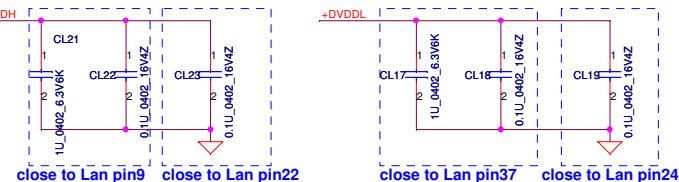
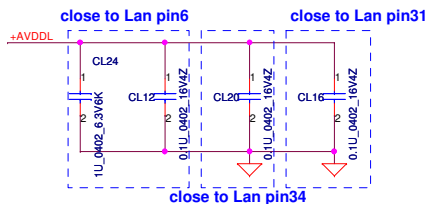
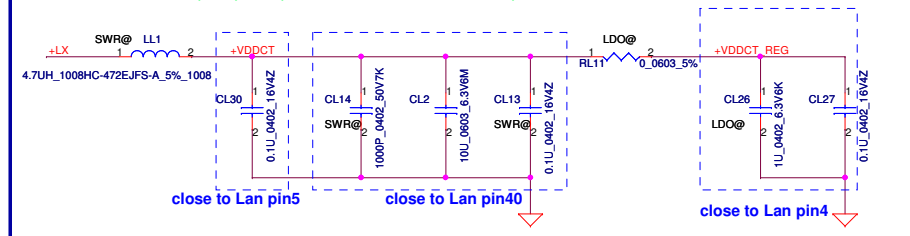


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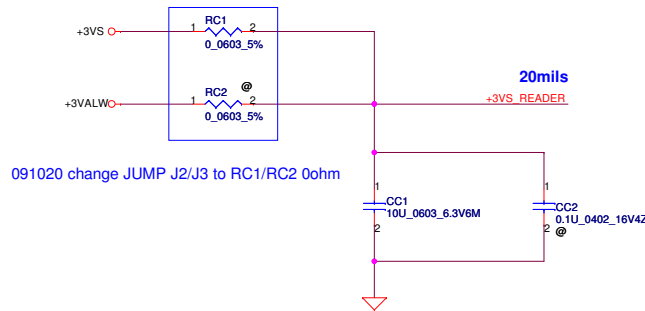
RL5 keep away other singal (25mil)

Mount CL30, CL2, RL11, CL26 and CL27. No mount LL1, CL14 and CL13.

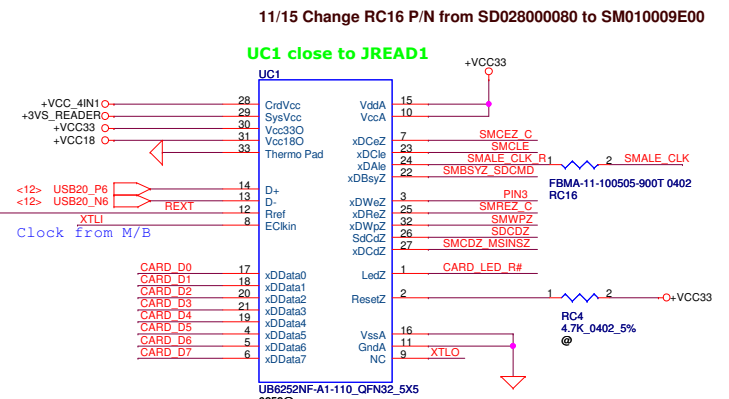


AR8152	Pin No.	PU/PD	Description
LED[0]	38	L	un-overclocking
		H	overclocking
LED[1]	39	L	LDO mode
		H	SWR mode

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				Custom	1.0
				Document Number P0VE6 Schematics	
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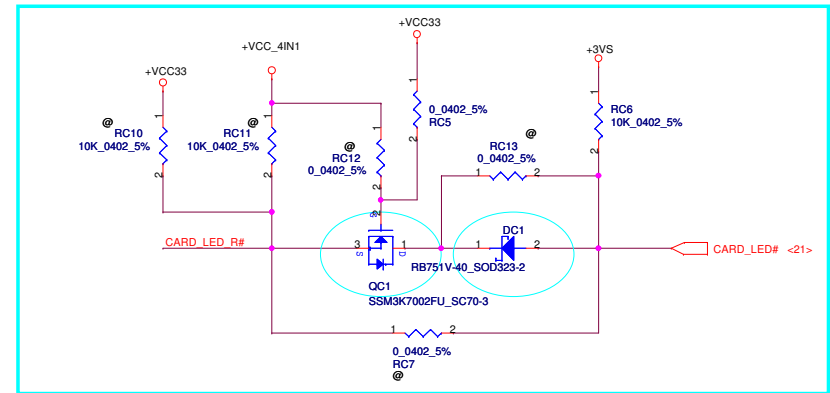
UC1
UB6250NF-A1-110_QFN32_5X5
SA00003FJ00
6250@
8/25 Co-lay UB6252 (6252@)



8/26 Change UC1 to UB6252 (SA00003K010)

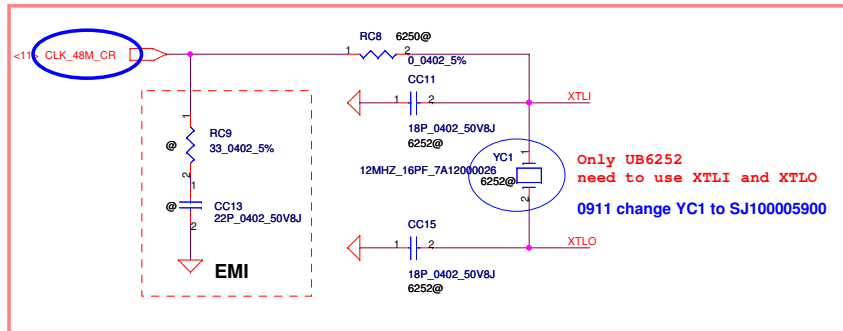
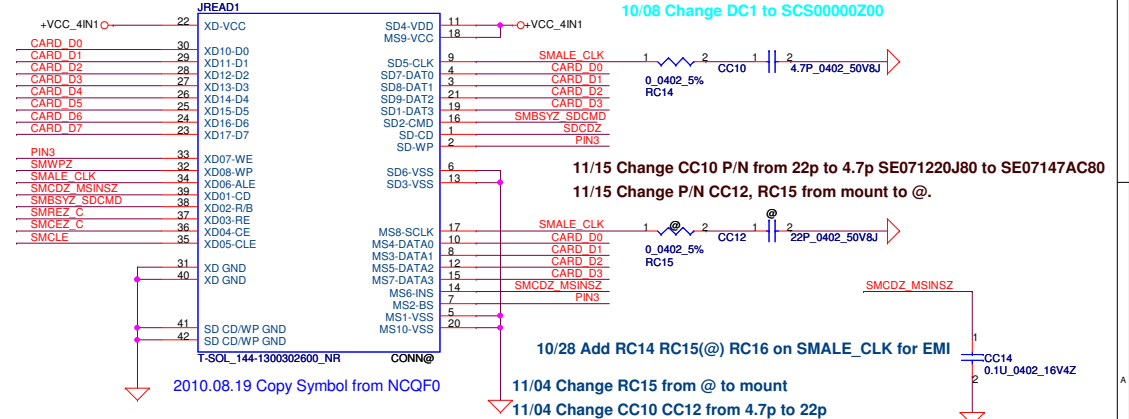
If use external crystal (YC1),
UC1 will change to UB6252

8/24 Card_LED# Follow PAV70

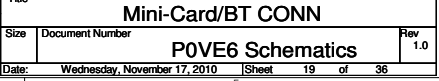


8/26 Change DC1 to SCS00002G00 Standard Part
8/26 Change QC1 to SB000009610 Standard Part
10/08 Change DC1 to SCS00000Z00

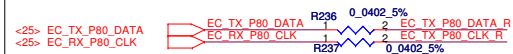
Card Reader Connector



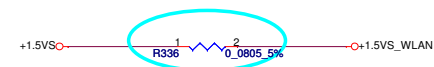
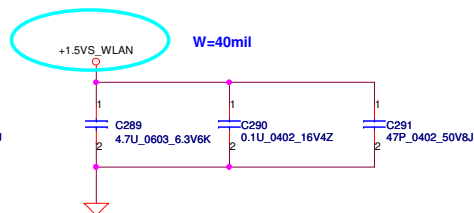
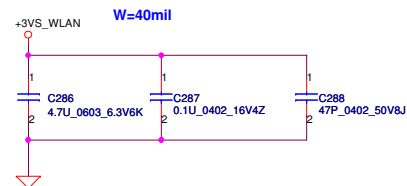
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Issued Date	2010/08/12	Deciphered Date	2012/08/12	CARD READER UB6250/6252	
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Mini-Express Card for WWAN

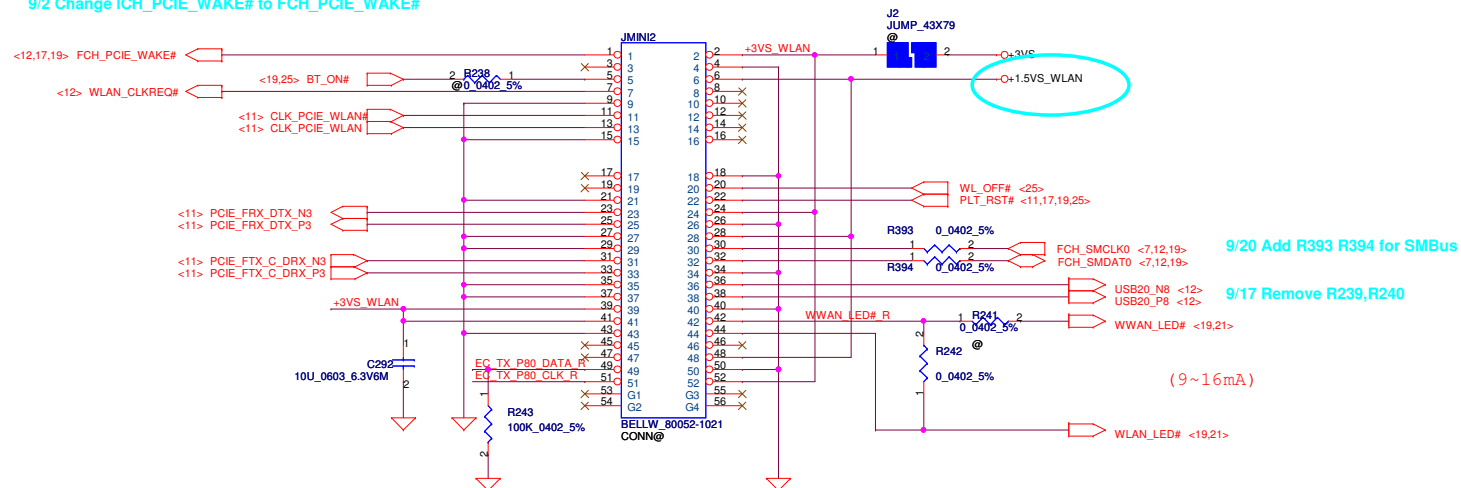


Mini-Express Card for WLAN



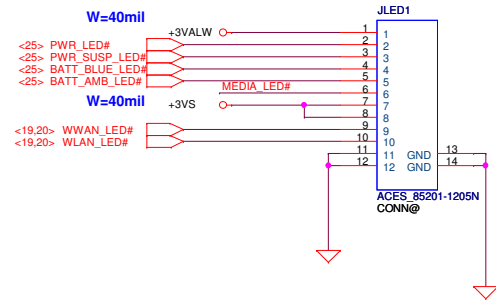
8/22 Reserve R336 (0 ohm 0805) Add net +1.5VS WLAN

9/2 Change ICH_PCIE_WAKE# to FCH_PCIE_WAKE#



5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

LED PCB CONN

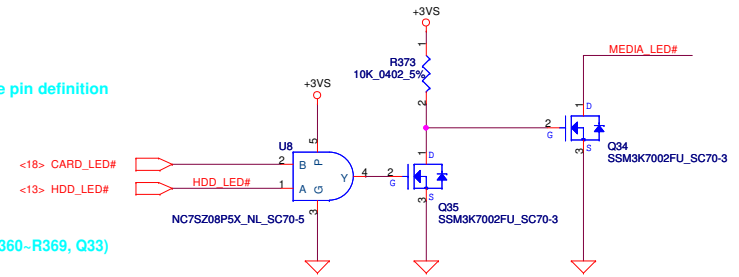


8/22 Update JP2 Symbol from database (ACES_85201-1605N_16P)

8/24 Update JLED1 Symbol from database (ACES_85201-1205N_12P) & Update pin definition

9/1 Add LED Circuit (LED2~4(SC597UDB000), LED5(SC5191NB000), R360~R369, Q33)

9/1 Change All LED power to 5V

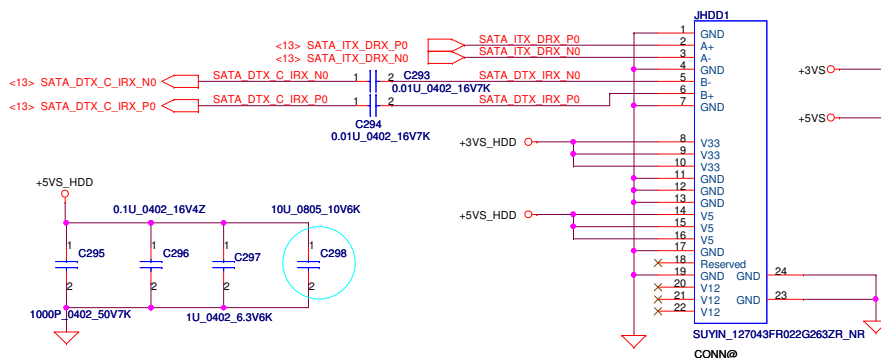


9/1 Add R373, Q34, Q35 for MEDIA_LED#

9/9 Change LED2~4 footprint to LED_HT-297DQ-GQ_4P

9/11 Remove LED portion

SATA HDD Conn.

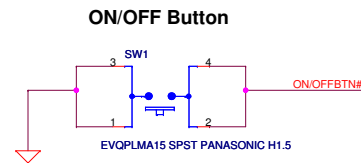


8/22 Reserve R337 R338 Add net +3VS_HDD,+5VS_HDD

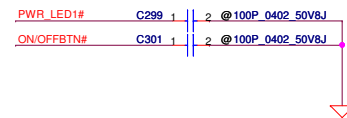
9/1 Change Q33 to SB000009610(SSM3K7002FU_SC70-3)

8/22 Change C298 from 10U 6.3V to 10U 10V

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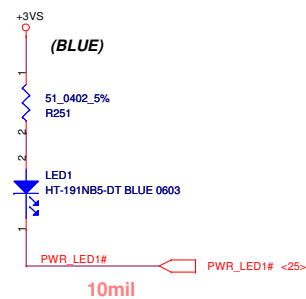
FOR EMI



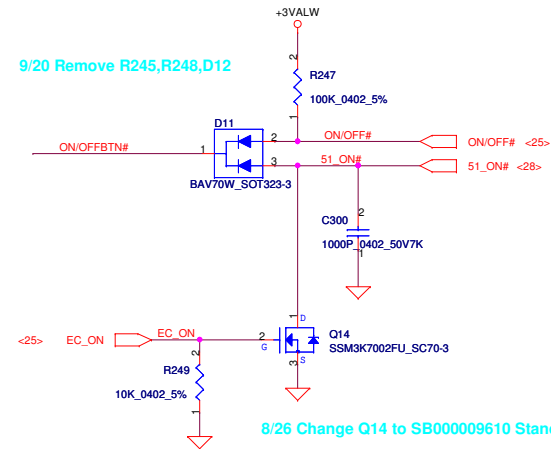
9/6 Change D13 from mount to @
10/05 Remove D13

9/1 Remove LED2 LED3 circuit, Change 70@ to mount

9/20 Add LED2 LED3 Circuit
9/21 Remove LED2 LED3 Circuit



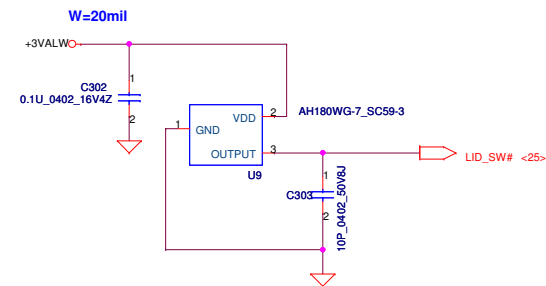
8/26 Change D11 to SC600000B00 Standard Part



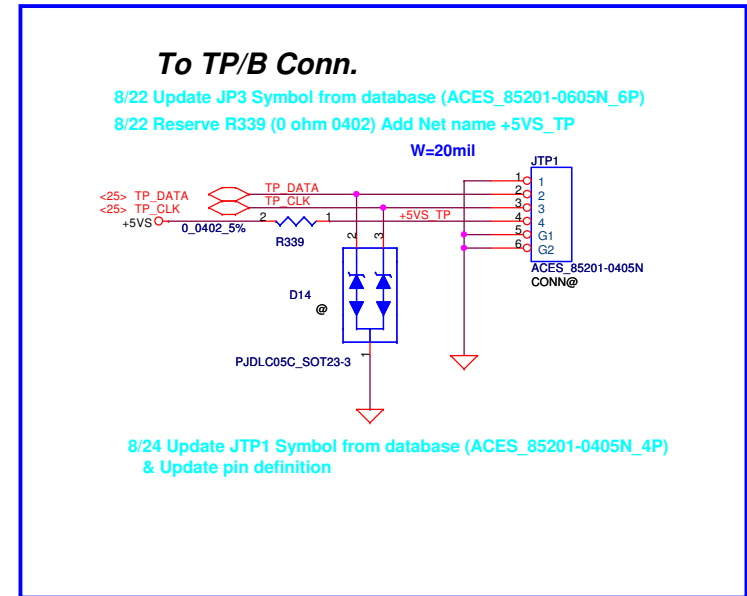
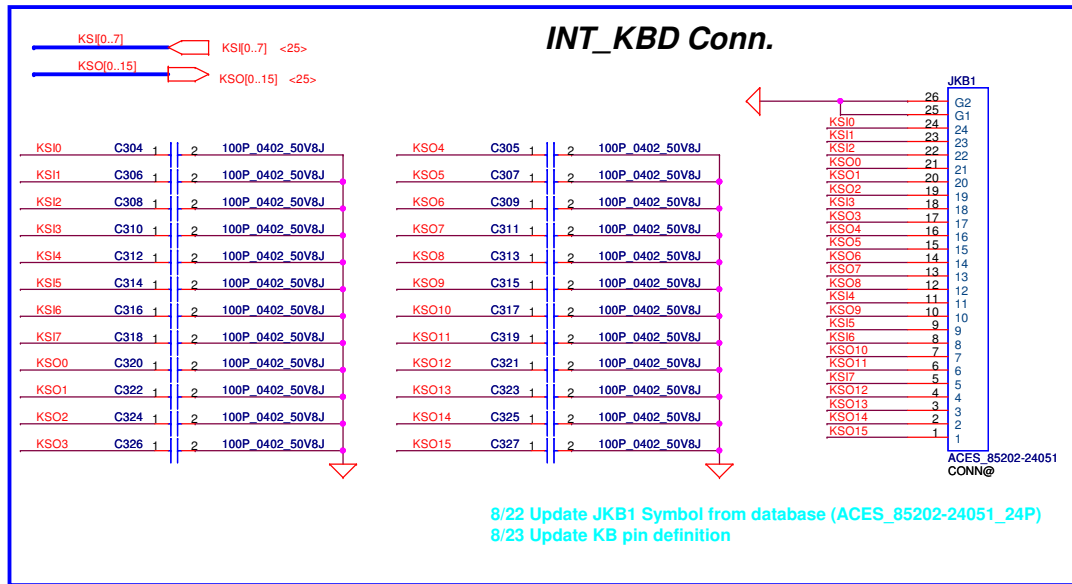
8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

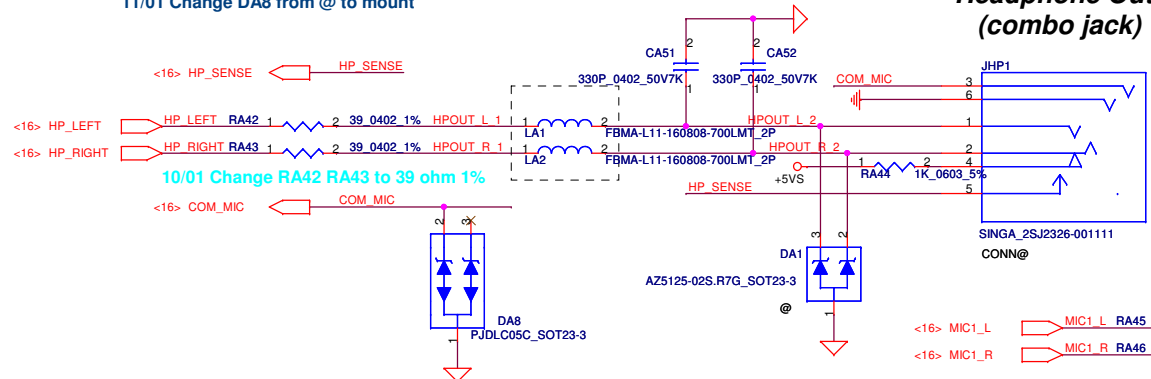
LID Switch



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11/01 Change DA8 from @ to mount

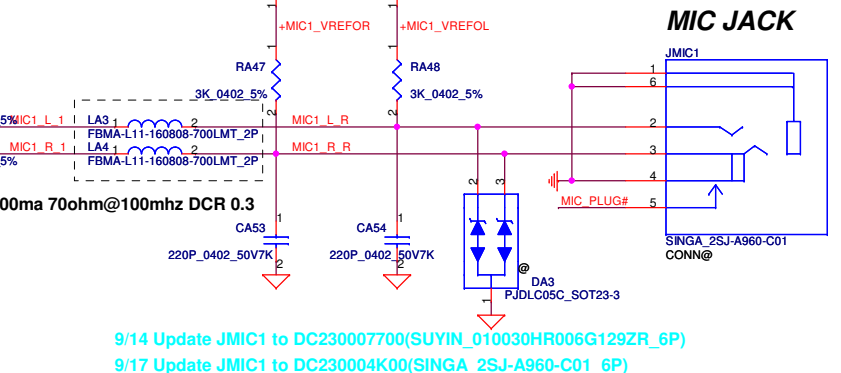


10/06 Change Jacks GND to GNDA

9/28 Change Jacks AGND to GND

9/13 Combine LS-7071PR01_USB_0908.DSN Audio Jack Portion

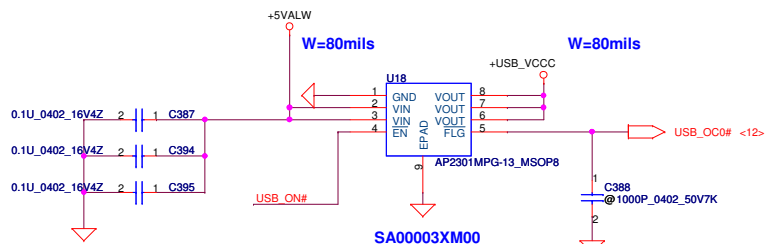
10/08 Change DA6,DA7 to SCS00000Z00



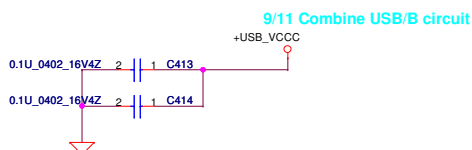
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Size	Document Number	P0VE6 Schematics		Rev 1.0	
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9/1 Add R370 R371 for OC circuit

9/15 remove R370 R371 for OC circuit



9/29 Add C394,C395(0.1U) Close to U18

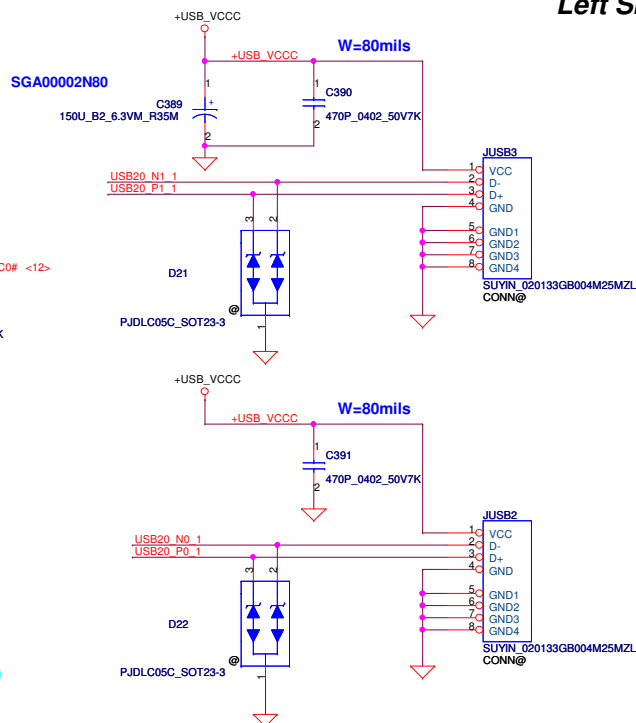


10/29 Add C413~C414(0.1U) on +USB_VCCC

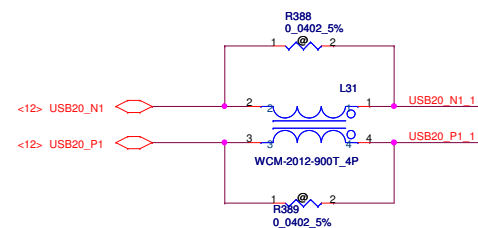
9/11 Change C340 C389 to SGA00002N80

9/24 Change U11,U18 to SA00003XM00

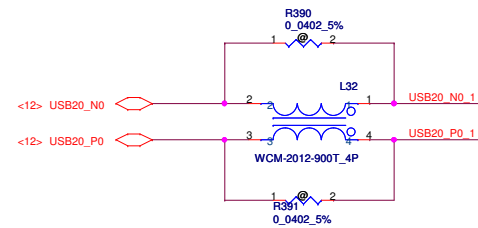
USB Charge Follow PAWGC
8/25 Remove Charge USB Circuit



Left Side USB CONN.



9/28 Swap L31 L32

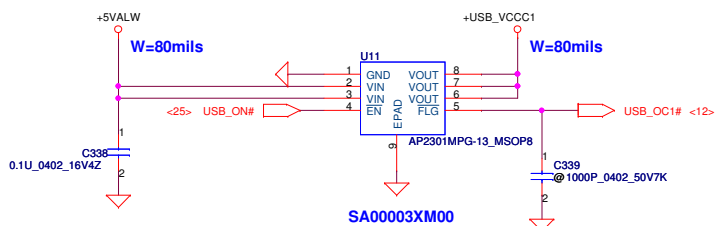


10/28 Change R388,R389,R390,R391,R257,R258 from mount to un-mount

10/28 Change L28,L31,L32 (SM070000K00) from un-mount to mount

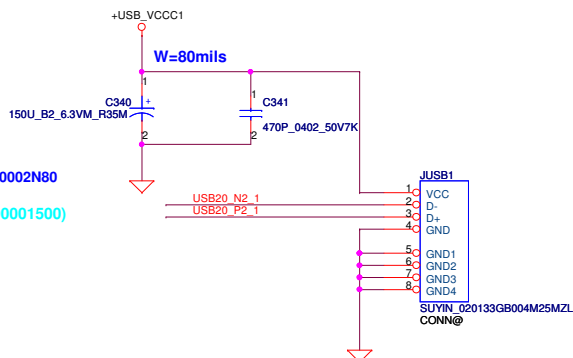
9/27 Change L28,L31,L32 to SM070000K00

Right Side USB CONN.

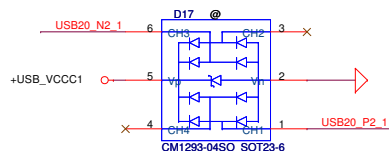
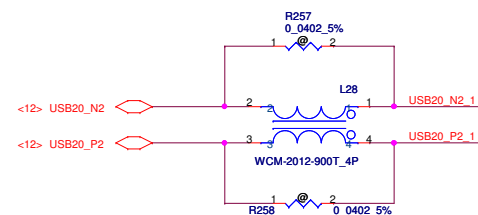


8/25 Change C340 from poly-cap to E-cap (SF000001500)

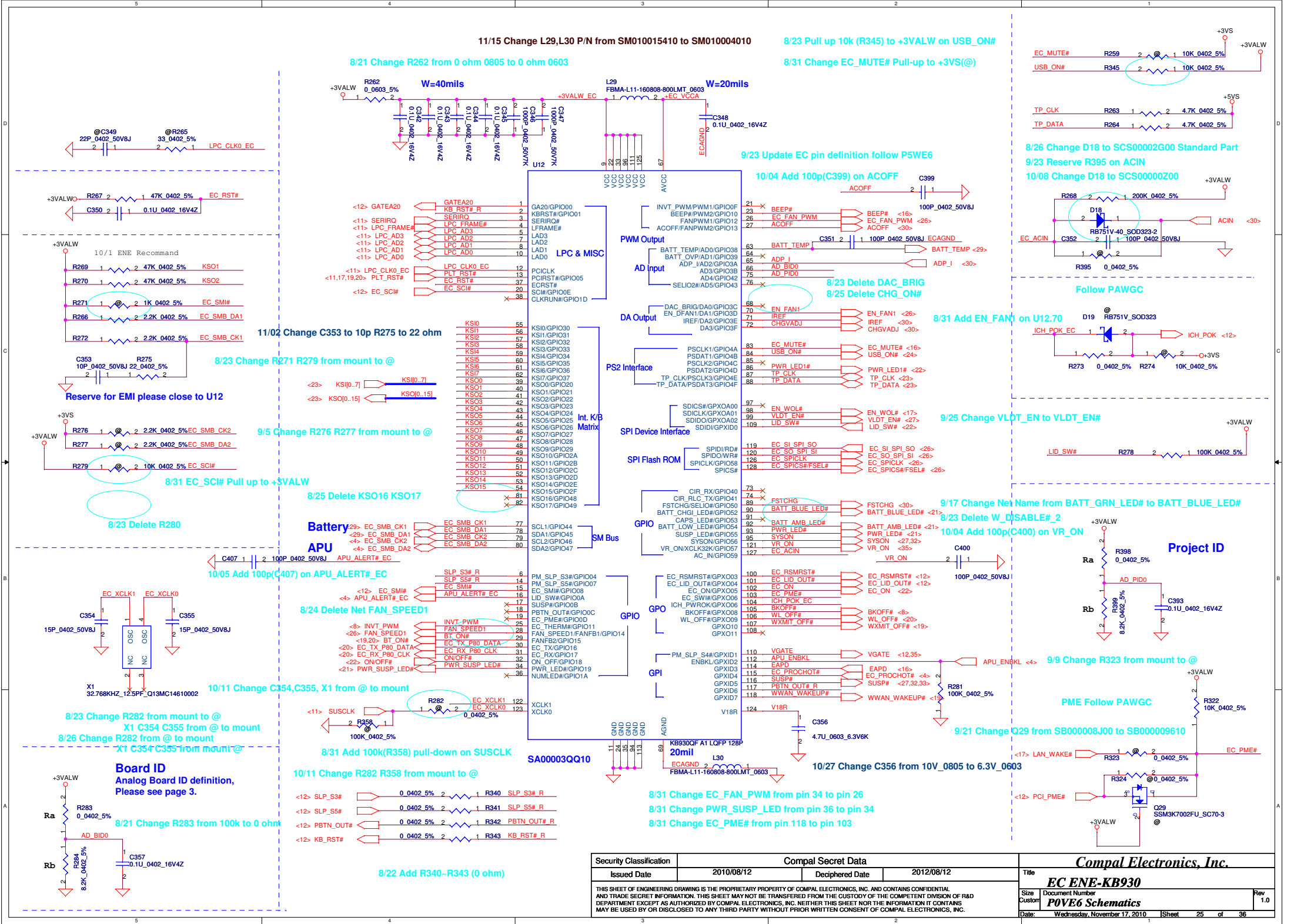
SGA00002N80



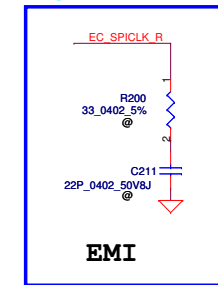
9/28 Swap L28



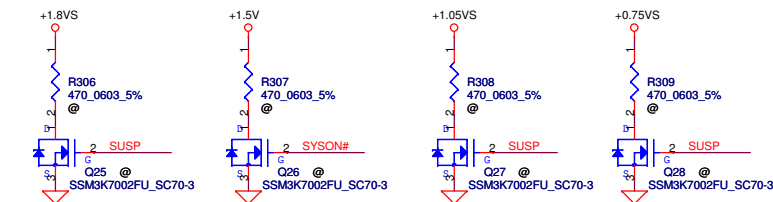
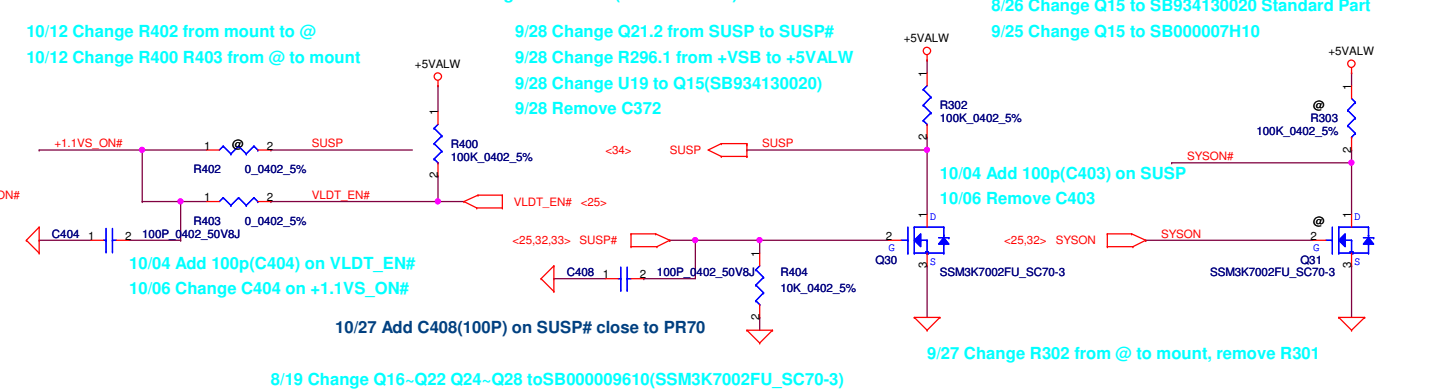
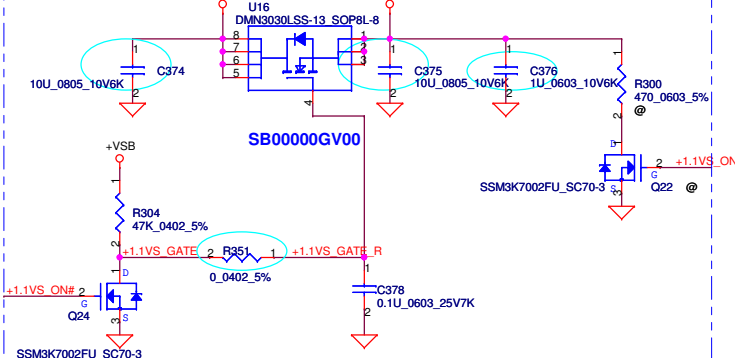
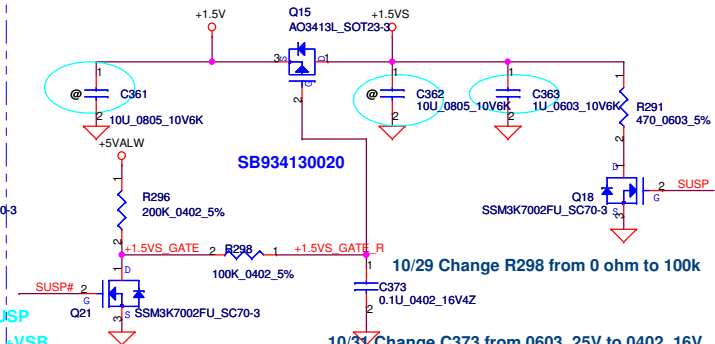
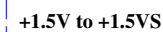
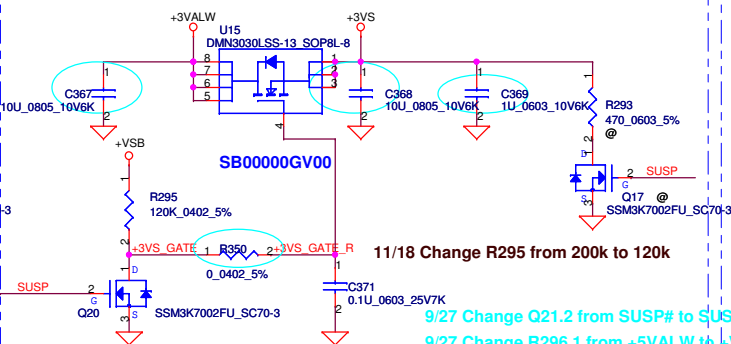
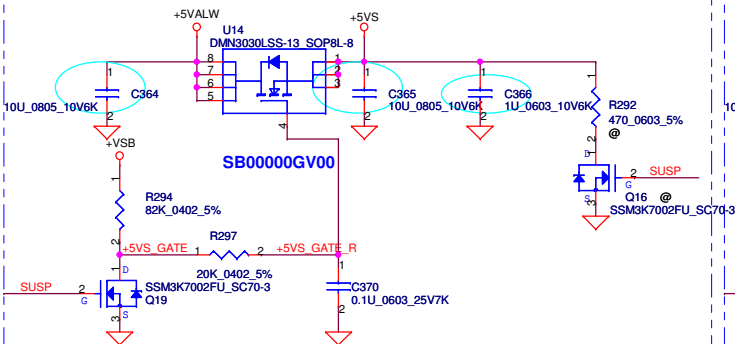
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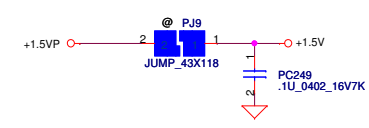
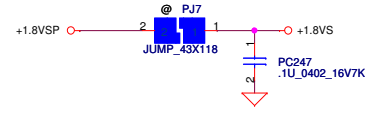
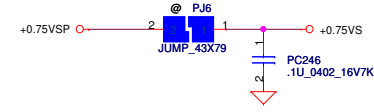
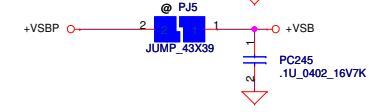
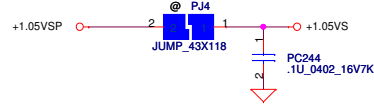
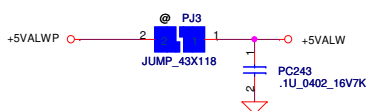
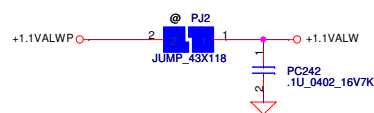
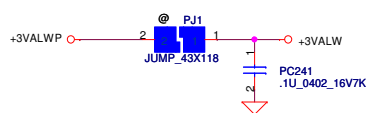
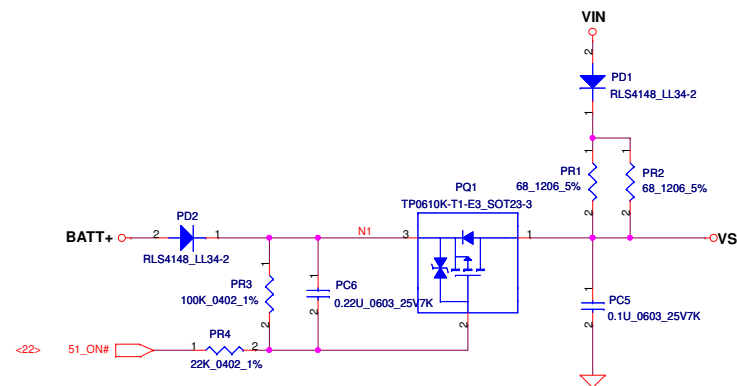
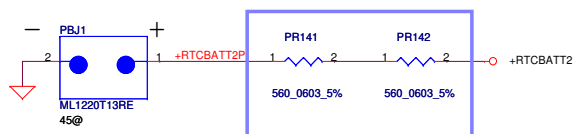
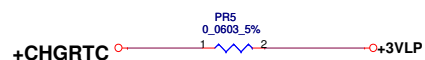
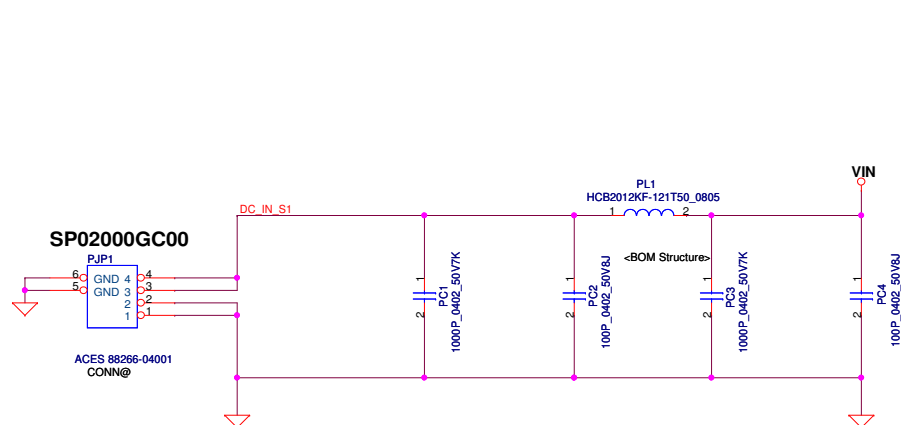
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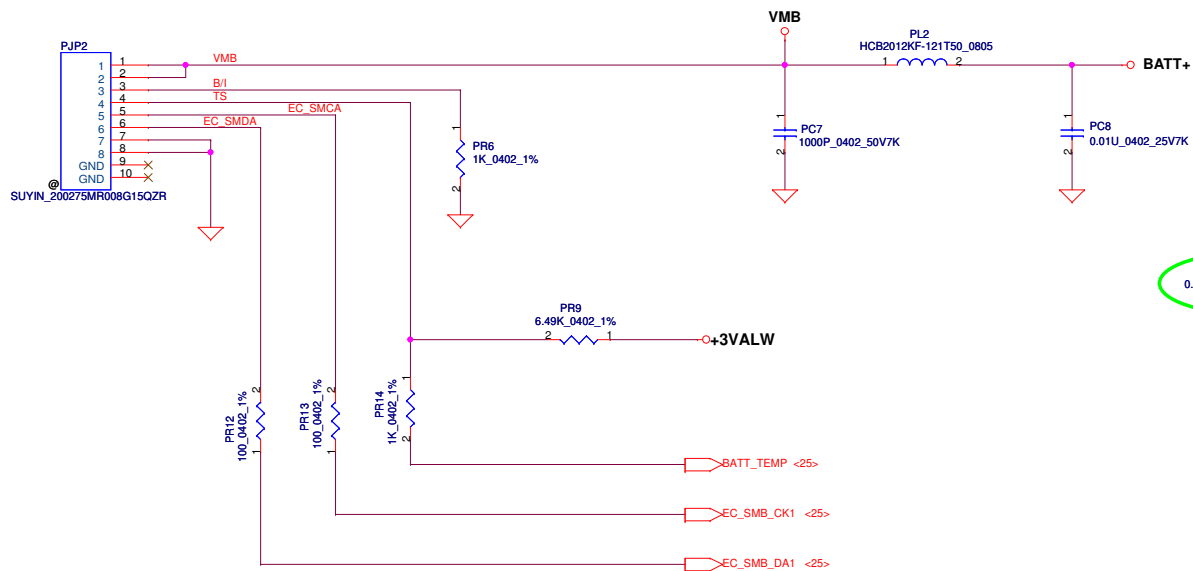
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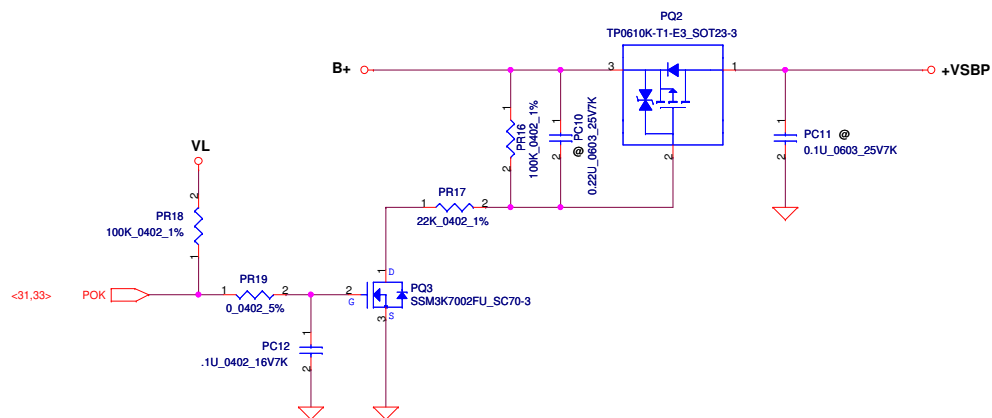
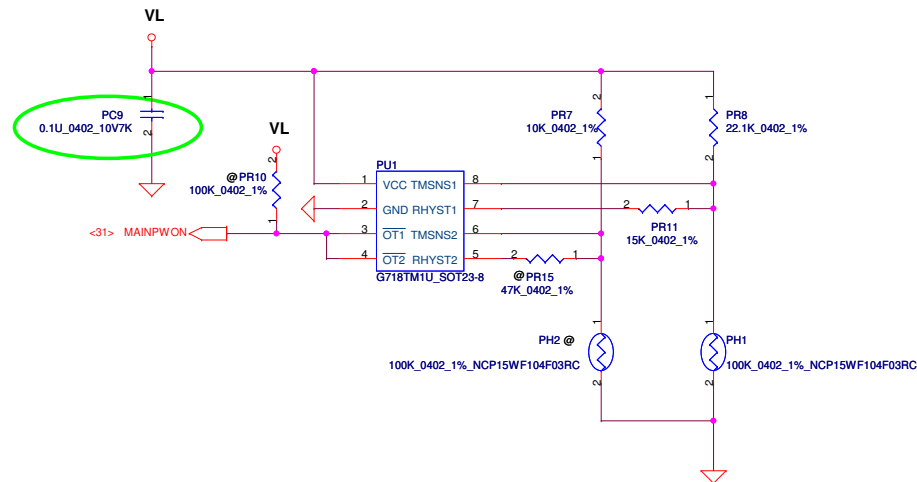
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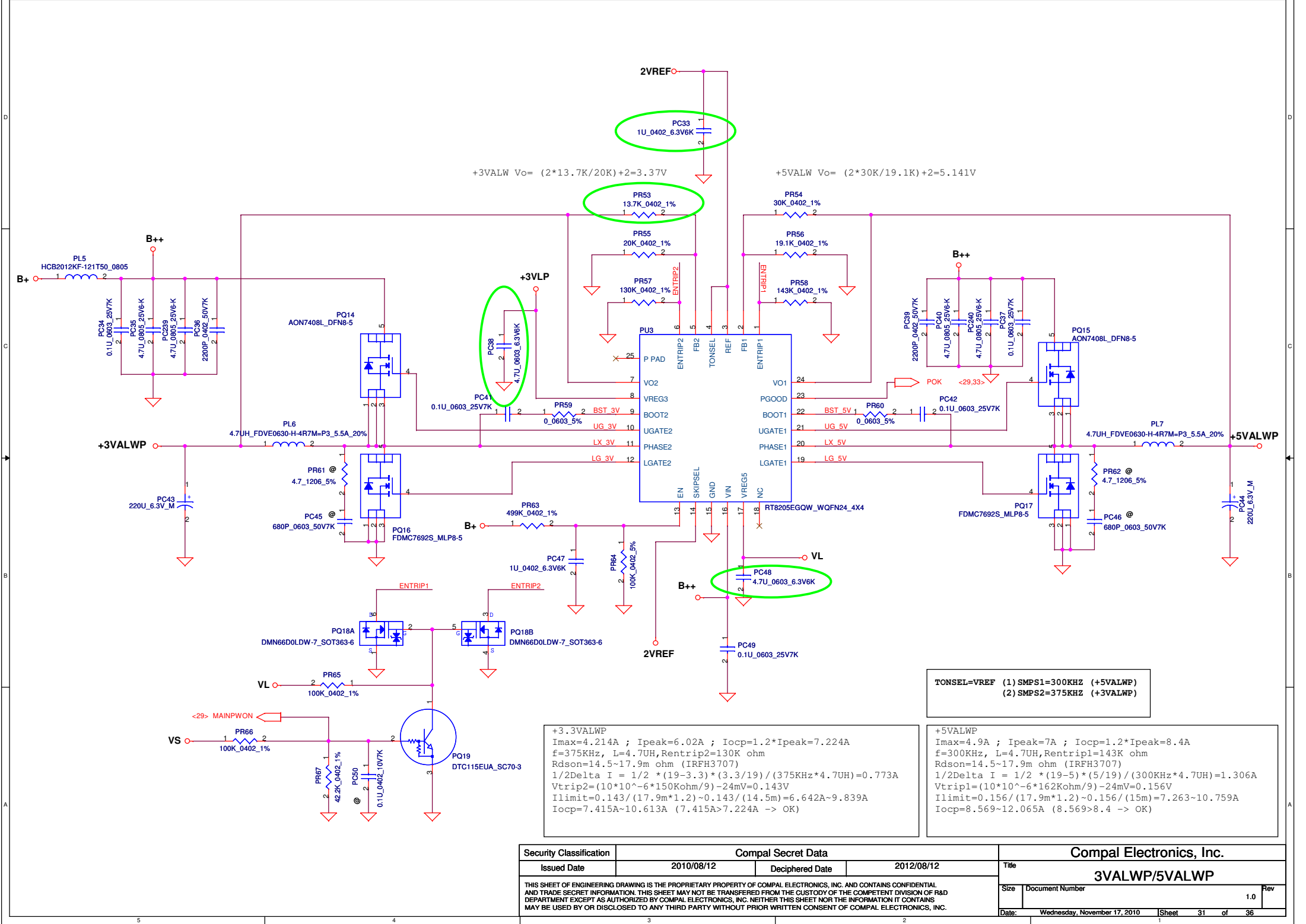
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



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+3VALW Vo= (2*13.7K/20K)+2=3.37V

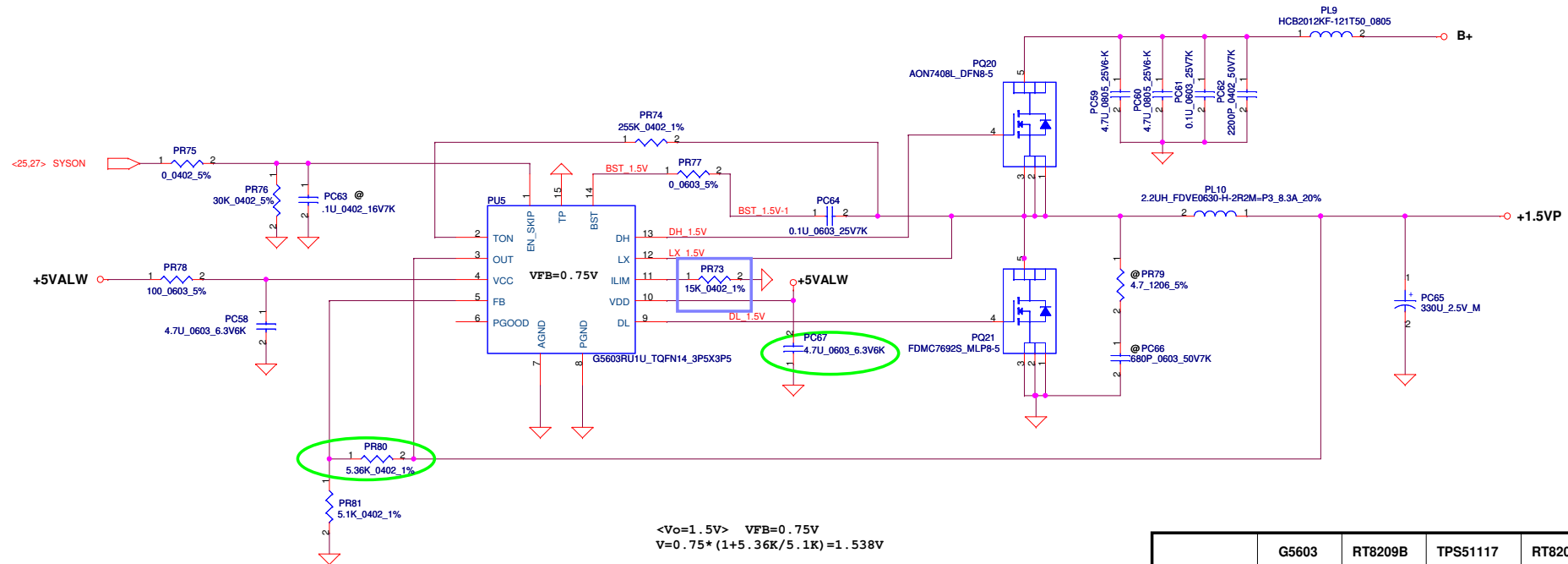
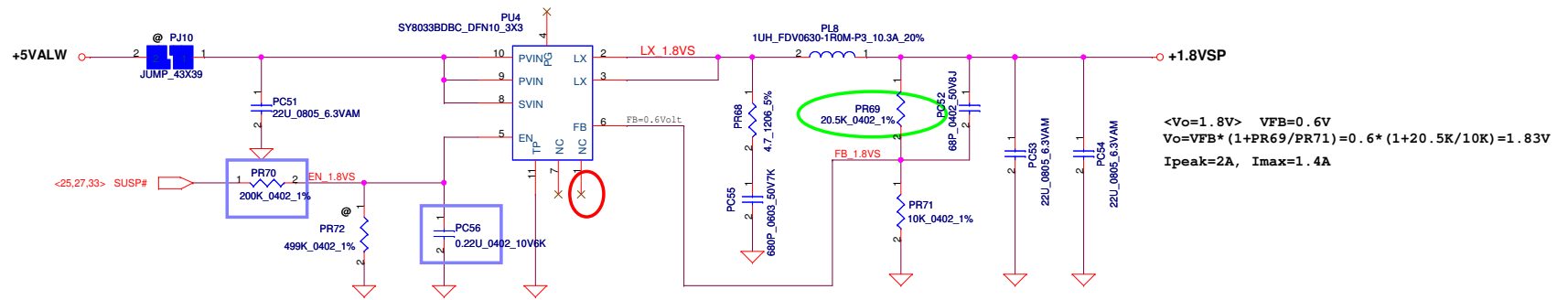
+5VALW Vo= (2*30K/19.1K)+2=5.141V

+3.3VALWP
Imax=4.214A ; Ipeak=6.02A ; Iocp=1.2*Ipeak=7.224A
f=375KHz, L=4.7UH, Rentrtp2=130K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 * (19-3.3) * (3.3/19) / (375KHz*4.7UH)=0.773A
Vtrip2=(10*10^-6*150Kohm/9)-24mV=0.143V
Ilimit=0.143/(17.9m*1.2)-0.143/(14.5m)=6.642A~9.839A
Iocp=7.415A~10.613A (7.415A>7.224A -> OK)

+5VALWP
Imax=4.9A ; Ipeak=7A ; Iocp=1.2*Ipeak=8.4A
f=300KHz, L=4.7UH, Rentrtp1=143K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 * (19-5) * (5/19) / (300KHz*4.7UH)=1.306A
Vtrip1=(10*10^-6*162Kohm/9)-24mV=0.156V
Ilimit=0.156/(17.9m*1.2)-0.156/(15m)=7.263~10.759A
Iocp=8.569~12.065A (8.569>8.4 -> OK)

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

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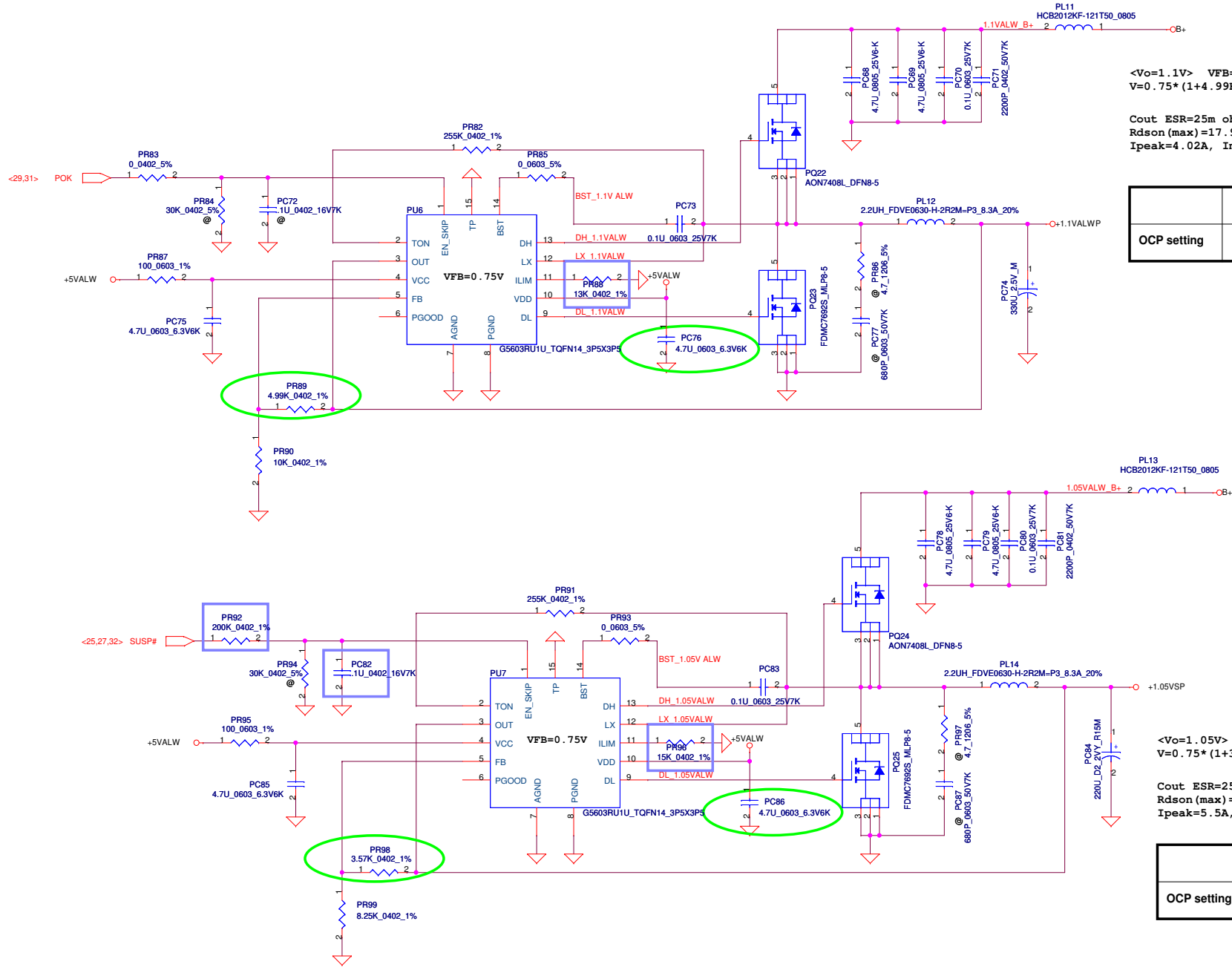


Cout ESR=25m ohm
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=6.5A, Imax=4.55A, Iocp > 7.8A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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$$\langle V_o = 1.1V \rangle \quad V_{FB} = 0.75V$$

$$V = 0.75 * (1 + 4.99K / 10K) = 1.124V$$

Cout ESR=25m ohm
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=4.02A, Imax=2.814A, Iocp > 4.824A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

$$\langle V_o = 1.05V \rangle \quad V_{FB} = 0.75V$$

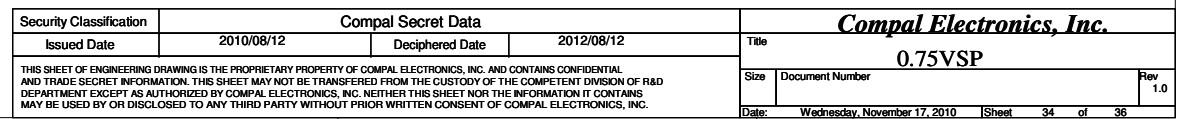
$$V = 0.75 * (1 + 3.57K / 8.25K) = 1.074V$$

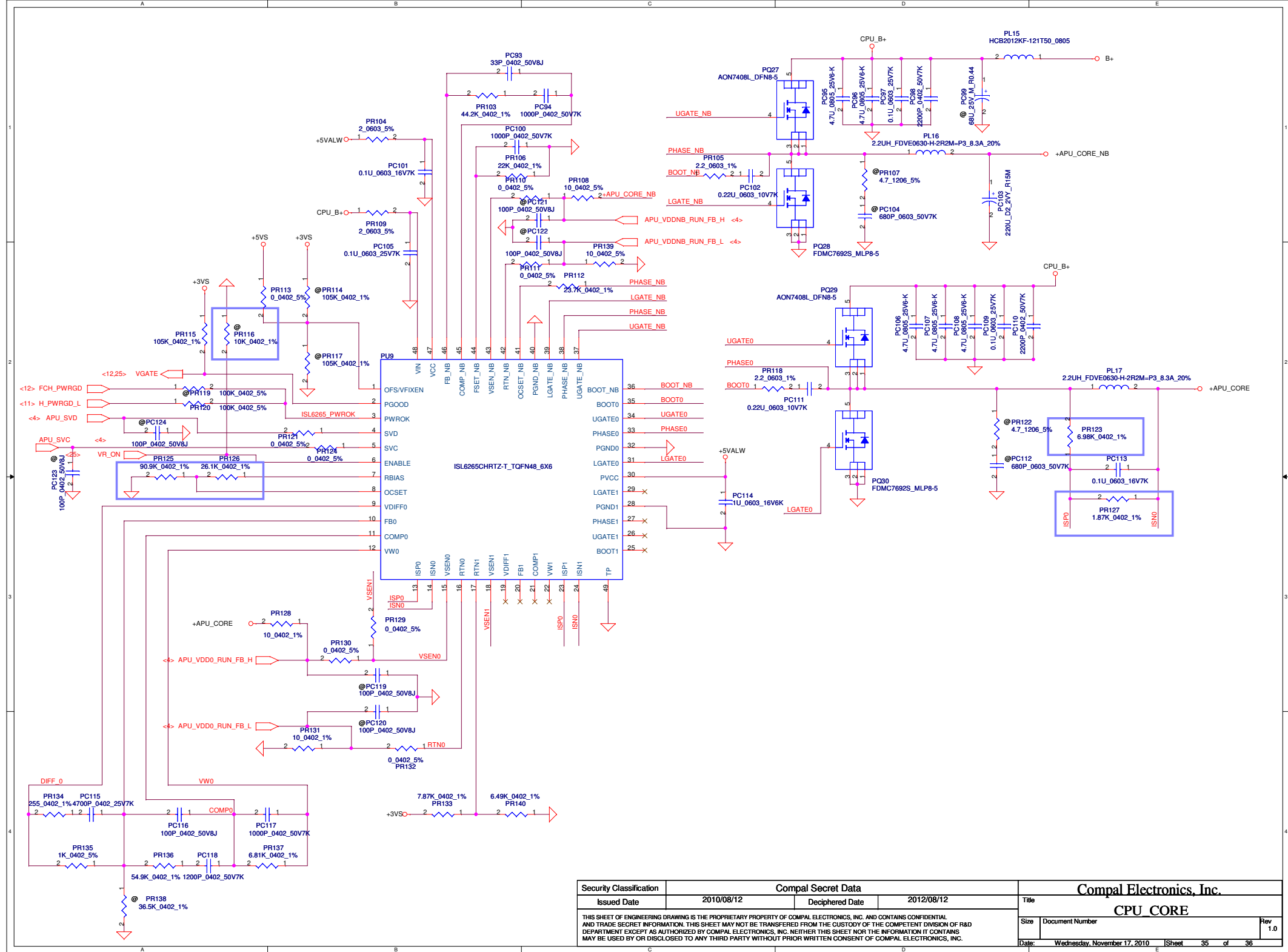
Cout ESR=25m ohm
 Rdson(max)=17.9m ohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=5.5A, Imax=3.85A, Iocp > 6.6A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify CP point for 40W adapter (40W*0.85=34W)	1	30	Change PR43 from SD034249280 (S RES 1/16W 24.9K +-1% 0402) to SD034470180 (S RES 1/16W 4.7K +-1% 0402)	20101011	EVT
2		Modify Outpot current sensor follow PAV70 design	1	30	Change PR38 from SD012200D80 (S RES 1/2W 0.02 +-1% 1206) to SD00000CI10 (S RES 1/2W 0.05 +-1% 1206)	20101011	EVT
3		Modify KI =1.62 follow PAV70 design	1	30	Change PR39 from SD034309380 (S RES 1/16W 309K +-1% 0402) to SD034620280 (S RES 1/16W 62K +-1% 0402)	20101011	EVT
4		Modify 1.5V OCP (there is only one dimm for 10.1")	1	32	Change PR73 from SD034787180 (S RES 1/16W 7.87K +-1% 0402) to SD034150280 (S RES 1/16W 15K +-1% 0402)	20101011	EVT
5		Modify 1.1V OCP for G5603	1	33	Change PR88 from SD034100280 (S RES 1/16W 10K +-1% 0402) to SD034130280 (S RES 1/16W 13K +-1% 0402)	20101011	EVT
6		Modify 1.05V OCP for G5603	1	33	Change PR96 from SD034140280 (S RES 1/16W 14K +-1% 0402) to SD034150280 (S RES 1/16W 15K +-1% 0402)	20101011	EVT
7		Modify +APU CORE OCP setting	1	35	Change PR123 to 6.98K ohm , PR127 to 1.87K ohm, PR125 to 90.9K ohm, PR126 to 26.1K ohm	20101011	EVT
8		+APU CORE power sequence concern	1	35	change PR116 to non-pop	20101011	EVT
9		Modify RTC schematic	1	28	add PR141 & PR142 =560 ohm	20101011	EVT
10		Modify SY8033B Enable pin pull down resistor	1	32	Change PR72 to non-pop	20101011	EVT
11		Modify 1.8VS power sequence	1	32	Change PR70 to 200K ohm , add PC56 =0.22uF	20101012	EVT
12		Modify 1.05VSP power sequence	1	33	Change PR92 to 200K ohm , add PC82 =0.1uF	20101012	EVT
13		Modify 0.75VSP power sequence	1	34	Change PR101 to 300K ohm , add PC92 =0.1uF	20101012	EVT
14							
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